The acronym EMC stands for "electromagnetic compatibility" and means the ability of an electronic device (or a module, printed circuit board or integrated circuit) to operate in an electromagnetically distorted environment while keeping its own distortions below certain thresholds so that other devices do not suffer any serious adverse effects.

For many people this field of expertise seems more like a form of black magic: No matter what work is done related to EMC, not only will something completely unexpected and unpredictable happen, worse than that it can be assumed that things will always take a turn in the wrong direction. It will become apparent through this article whether this viewpoint is accurate and what engineers can do to gain more facility in this field.

Those involved in the field of electronics, especially in the automotive sector, will certainly have been confronted by EMC-related issues more than once. The phenomenon of radio interference is nearly as old as the invention of radio itself and at an early stage led to the definition of guidelines for noise suppression. The other part of EMC, the immunity against distortions, only began attracting attention around fifty years ago. While it is merely a nuisance to experience radio interference, it is definitely a serious matter if an ABS or airbag may also be affected by interference, e.g., when passing a TV tower. Not only is the number of electronic control units in cars on the rise, so too is the number of electronic devices frequently used inside the cars such as cellphones, portable navigation devices, wireless headsets which may also cause interference. Making matters even worse is that more and more of devices of this kind operating at higher and higher frequencies are constantly being introduced to the market. Higher frequencies imply that smaller structures can behave like an antenna and cross-coupling needs to be considered even for relatively small coupling capacitances. It is therefore only natural that there has been a growing need to define certain rules of the game over the past decades.

Today all car manufacturers are aware that EMC testing is an important part of car electronics development and understand that EMC issues become costlier the later they are discovered. That is the reason why they do not just rely on a final test inside the car but insist on tests of the electronic control unit (ECU) and even on test results of the integrated circuits used in the design before deployment in vehicles. All around the world a wide variety of test methods have been developed for both unwanted electromagnetic emissions as well as the susceptibility for electromagnetic distortions. In the meantime, all integration levels are covered and over the past 10 years the various standardization committees have devoted their time to the IC level. As a semiconductor manufacturer, Atmel is confronted primarily with IC-level and ECU-level tests. Unfortunately, not only have there been quite a large number of different standards established (perhaps a bane to testing specialists), at the same time, many OEMs apply these standards in slightly different ways.

Two different types of measurements can be distinguished in the case of emission as well as susceptibility tests:

- The radiated measurements, involving an antenna, a coupling clamp, a magnetic or electric probe, a stripline or a TEM cell
Measurements carried out using galvanic coupling to certain ports to measure or inject RF signals

Semiconductor companies have to deal mostly with testing at the IC level, however certain applications such as automotive networking systems also require the proof that some module level tests are passed by those ICs that include integrated bus line transceivers. The “classic” EMC tests at the IC level measure the emissions in varying frequency bands at defined frequency steps, dwell times, measurement bandwidths and detector types as well as measuring immunity by applying an unmodulated or AM-modulated RF signal of defined amplitude, again while varying the frequency at defined steps. These tests are specified in the international standards IEC 61967 for emission and IEC 62132 for immunity. Currently these standards are supplemented by new test standards for pulse measurements.

Most ports at the IC level are designed to be connected internally on the PCB only while just a few ports, such as supply pins, bus lines or antenna pins, are connected externally. While EMC requirements are less stringent for local (internal), the global (external) ports are far more critical because the cable lengths involved increase the cross-coupling between different lines or may behave as an undesired antenna for RF signals. Certainly a few ports such as those for bus lines are external ports by definition, but for most ports it is the application that determines whether they need to be treated as local or global ports.

The good news is that designing circuits and board layouts which are robust will not only ensure an assembly works better and is more dependable but in most cases also help to achieve the required performance regarding both electromagnetic emissions and immunity. Having said this, how can circuit design be achieved which is that robust? Of course there are a few general rules which help to improve the EMC behavior of the circuit:

- Careful consideration should be given to what clock frequency is really needed for the development application. The lowest clock frequency possible should be chosen because this is the first measure which will reduce electromagnetic emissions.

- High-impedant ports are susceptible to RF distortions; therefore, impedance should be kept as low as acceptable or a low-impedance path to GND for the RF disturbance should be provided. If an integrated circuit indicates that some GND pins are related to certain VCC pins or ports, where decoupling caps are placed should take this knowledge into account. Ports that are connected on the outside of the ECU require special attention – plan for decoupling capacitors to GND and series resistors if possible – 10 to 100Ω are often acceptable, whereas higher values will form a more efficient filter but also cause a higher voltage drop for DC signals. If emission of a particular port is the problem, one end of the resistor is connected to the port while the capacitor is on the other side. To protect a port against RF distortions the components are arranged inversely. For frequencies >10MHz ferrite beads may be more efficient than only utilizing small resistors and as a further benefit their DC resistance is negligible, meaning the circuit will not suffer from a drop in voltage.

- For higher frequencies a capacitor functions not only as a capacitor but also has some inherent, built-in parasitic components such as series inductance and resistance – known as equivalent series resistance (ESR) – to name only the most important components with adverse effects. Because the correct choice and placement of decoupling capacitors is of vital importance, this will be discussed in more detail below.

- In addition, resistors need to be regarded as a more complex component (highly depending on the type of construction and also on the resistance value). Fortunately, for a typical low-ohmic thin film resistor as they are used for building EMC filters, the contribution of its parasitic components is largely negligible up to 1GHz.

- When developing the PCB layout, the different circuit blocks should be arranged in such way that sufficient space around sensitive inputs is provided towards switched signals of high amplitude and/or frequency because of the possible interferences these signals may cause. Having parallel tracks on a board provides good coupling between the signals on these tracks – if this kind of coupling is not desired, insert some GND area between the tracks; should these tracks cross each other at different layers, have the tracks cross at right angles to minimize the coupling area. Keep tracks as short as possible, especially those carrying RF or switched signals with fast slopes. Critical parts of the circuit such as tuners may require shielding. The highest frequency the circuit produces or is exposed to should be considered and the track length of critical connections kept below 1/10 of the wavelength. Two considerations must be kept in mind here: First, the...
wavelength $\lambda$ on the PCB is shortened due to $\varepsilon_r$ of the board material, for FR4 this is typically around 4.5; however the effective $\varepsilon_r$ will be somewhat lower because part of the electric field of a micro strip line is in free space. For a frequency of 3GHz the formula

$$\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_r}}$$

reveals that a track length of about 50mm already equals $\lambda/10$.

Secondly, the highest frequency in the circuit is determined by the fastest slopes – so if some parts of the design operate at 1MHz but with slopes of 1ns, there will be frequencies of at least 500MHz on the PCB.

- Differential signals must be routed close to each other with the same track length for both lines. Avoid generating large loops and keep the path for the return current in mind. The larger the area of a loop, the higher the susceptibility and the lower the frequencies which may impact the circuit. Analogously, this is valid for emission, too – any tracks forming a loop with an RF current flow can behave like a loop antenna.

- The ground plane should be designed as solidly as possible, preferably using a multilayer PCB with dedicated layers for GND and power planes. Typically, the signal layers will be on the top and bottom side of the PCB and the GND/power planes on the inner layers. It is advantageous to keep the distance between signal layer and adjacent GND/power plane to a minimum. Doing so helps achieve relatively low track impedance even for fairly thin connections. Slots in the GND plane should be avoided to prevent creating unwanted slot antennas. In addition, small “islands” should be avoided, different GND areas need to be connected using a sufficient number of vias (one via every 3 to 5mm is sufficient for most designs).

- Hopping between the layers should be kept to a minimum during board development. Every via, especially “long” ones from top to bottom layer, involve some inductance; as a rule of thumb this is in the range of 0.5 to 1nH. Particular care needs to be taken about GND connections of decoupling capacitors. Atmel® highly recommends placing several vias in parallel close to the respective capacitor.

**Equivalent Circuit Model of the Capacitor**

In the capacitor’s equivalent circuit model, the simplest model comprises just a serial connection of the nominal capacitor, an equivalent series resistance and a parasitic series inductance. The ESR determines the lowest impedance reached at the capacitor’s series resonance. Above this series resonance the capacitor’s impedance will increase with frequency, thus behaving like an inductor. A more sophisticated model would also include the components $C_p$ and $R_p$ connected in gray in Figure 1. Modified equivalent circuits are also found in literature which show $C_p$ and $R_p$ in parallel to the whole serial connection of (desired) capacitor, ESR and parasitic inductance; it is merely a question of transforming the values of the respective inherent components. The parasitic inductance together with $C_p$ leads to a parallel resonance that is frequently neglected, because such parallel resonance of typical SMD ceramic capacitors will only appear at several GHz.

The series resonance of the capacitor is determined by its type (electrolytic, foil, ceramic), mechanical dimensions (axial, radial, SMD, size) and of course its value. The higher the capacitance of a certain capacitor type, the lower the series resonance frequency. Therefore, it is advisable not just to place a single capacitor for decoupling purpose, but combine two or several caps to achieve broadband decoupling. For example, it is often recommended to pair a
10nF capacitor for lower frequencies with a 100pF cap for higher frequencies. The following will explore whether this is advisable. A very basic linear RF simulation tool is sufficient for demonstrating this; there are even freeware tools available for this purpose. Many manufacturers of ceramic capacitors supply S-Parameter files for their products and it is advisable to use them. Figure 3 shows the attenuation of the above two capacitors when placed in parallel from a 50Ω track to GND.

This looks quite acceptable. Attenuation of at least 30dB was achieved for frequencies between 20MHz and well above 1GHz. If a higher reference impedance than 50Ω had been used, it would look even better. In a rather ideal world, it would be possible to stop here. But has something been overlooked? In reality, it is not possible to connect the capacitors perfectly to GND or to the track or pad which needs to be decoupled. Every track on the PCB above behaves like a transmission line and its impedance is determined primarily by track width, the thickness of the PCB or, in case that a multilayer PCB is used, the distance between signal and GND layer, the distance to adjacent GND areas and the dielectric constant \( \varepsilon_r \) of the PCB material. Again, there are special books and free calculation tools available for guidance on this issue. With track widths of 0.2mm, GND area >0.5mm away from the track and \( \varepsilon_r = 4.7 \), impedance of well above 100Ω for 2-layer boards (1.6mm standard thickness) will result and close to 50Ω will result for a multilayer board with 150µm distance between signal layer and GND plane.

When considering the red curve in Figure 4, it is obvious it looks quite different from the previous graph. Figure 4 shows how decoupling performance changes if the board layout is not done with care. The assumptions for the red curve were as follows: standard 2-layer PCB, distance between caps and to their GND vias: 10mm with just one GND via per cap. Now, quite unexpectedly, there is a highly undesirable resonance around 130MHz with attenuation of only 6dB. The green graph in Figure 4 shows the performance for an improved board layout. Now a multilayer board is used, the two caps are closer to each other and each one has two GND vias only 1mm away from the respective cap. The resulting decoupling performance is significantly improved, but there still seems to be room for improvement.

The lesson learned from this example is, first, the decoupling caps need to be as close as possible to each other and to the component which needs to be decoupled. Secondly, using a multilayer PCB with a GND plane just below the signal layer is beneficial too. And, finally, it appears to be a good idea to do some simulation with “real” capacitors rather than just

![Figure 3. Attenuation of two Ceramic Capacitors of 10nF and 100pF in Parallel in a 50Ω System](image)
selecting them based on instinct. Innovative layout designs even place only a single centralized group of capacitors to decouple a larger area – but that is something which should not be attempted without careful simulation.

As mentioned previously in this article, car manufacturers are aware that EMC issues generally become costlier the later they are discovered. Engineers may benefit from this insight within their own development work. Giving some thought to EMC behavior already when designing a circuit definitely helps avoid unpleasant surprises during EMC approval testing. Having said that much – what needs to be done if a design fails EMC testing despite the care exercised prior to testing? Or, just in case it was not possible to include sufficient time, budget or experience appropriate for EMC assessment in a project, what can be done to improve matters?

The truth is that no standard procedure exists. If emission is the problem, a probe across the circuit can be attempted with a field probe to detect any potential “hot spots.” Or, if fast enough, it is possible to re-perform the particular failed emission measurement while connecting a short isolated wire to some “suspicious” spots on the PCB. If a critical one shows up, the number of spurs will increase; this becomes immediately noticeable on the connected receiving instrument. If the design performs weakly in terms of susceptibility, consideration must be given to what parts of the circuit are affected (this can often be deduced from the malfunction occurring during the immunity measurement), and the coupling path must be located. Once the critical parts of the circuit have been pinpointed, the techniques described above can be used to improve EMC performance.

A key consideration in this regard is that effective decoupling requires a solid GND area. If this is lacking, it may be easier to redesign the board first; alternatively some copper foil could be added to facilitate further optimization measures in the lab.

Hopefully it has become apparent that there is nothing magical at all about EMC and that it is simply applied physics. Naturally, our knowledge about coupling mechanisms and particularly their parameters tends to be inaccurate and sometimes incomplete, even if highly sophisticated electromagnetic simulation tools are used. So there is a trace of magic (or uncertainty) left in the process after all. But these imponderables are also what challenge us daily in this specialized discipline.

---

**Red:** Distance between caps and their GND vias: 10mm, one GND via per cap, track width: 0.2mm, board thickness top to GND: 1.6mm.

**Green:** Optimized, distance between caps: 5mm, between caps and their GND vias: 1mm, two GND vias per cap, track width: 0.2mm, board thickness top to inner GND plane: 0.15mm

---

Figure 4. Attenuation of two Ceramic Capacitors of 10nF and 100pF in Parallel in a 50Ω System with Realistic Parasitic Components in Connecting Tracks