APPLICATION NOTE

AT01084: XMEGA E Using the XCL Module

Atmel AVR XMEGA E

XCL Features

- Two independent 8-bit timer/counter
- One 16-bit timer/counter by cascading two 8-bit timer/counters
- Programmable lookup table (LUT) supporting:
  - AND, NAND, OR, NOR, XOR, XNOR, NOT, MUX
  - D-Flip-Flop, D Latch, RS Latch
- Input sources:
  - From external pins or the event system
  - USART pins
- Outputs:
  - External pins or event system
  - USART pins

Introduction

XCL (XMEGA® Custom Logic) is a new module available on the Atmel® XMEGA E family. This document describes the XCL module from the application side with answers to common questions.

The datasheet gives a complete and accurate description of XCL module. All functional modes are described and it is sometimes difficult to extract a simple/common mode to understand the benefit of using XCL.

This document presents datasheet extracts with a focus on important parameters and explanations on XCL usage. Schematics are often simplified to high light the important features.

XCL is linked to clock system, UART, Event system, and I/O ports.

Table of Contents

1. Definitions

Name	Description
XCL	XMEGA custom logic
LUT	Lookup table including truth table register and decoder
BTC	Byte Timer Counter
PEC	Peripheral Counter

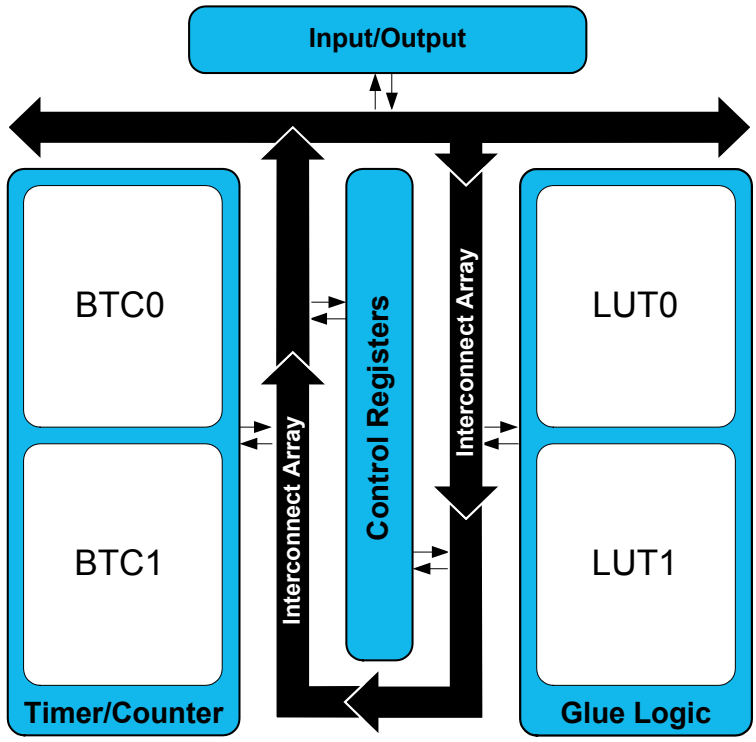
2. XCL Overview

The XCL module is made of two major sub-units:

- Two 8-bit timer/counter (BTC0, BTC1)
- Two configurable Look Up Table (LUT0, LUT1)

Independent usage of LUT and timer/counter is possible.

The XCL module interacts with UART and EVENT modules.



3. LUT Description

3.1 Overview

XCL includes two lookup table units (LUT). Each LUT is composed by a 4-bit truth table and a decoder.

LUT allows generation of any logic expression with two inputs and one output.

Cascading LUT0 and LUT1 is possible to obtain a logic expression with three inputs.

Sequential logic functions are available on LUT output (D-FlipFlop, D Latch and RS Latch).

Delays on LUT input/output can be used to synchronize/filter LUT signals.

3.2 Features

Programmable lookup table supporting multiple configurations:

- Two 2-input units
- One 3-input unit
- RS configuration
- Duplicate input with selectable delay on one input
- Connection to external I/O pins or event system

Combinatorial Logic Functions using programmable truth table:

- AND, NAND, OR, NOR, XOR, XNOR, NOT, MUX

Sequential Logic Functions:

- D-Flip-Flop, D Latch, RS Latch

3.3 LUT Definitions

Name	Description
LUT	Lookup table including truth table register and decoder
DLY	Delay element, created with a programmable number of flip-flops. Position is selectable by software, between one LUT input or LUT output
GLUE	Glue logic, including a LUT and DLY elements

3.4 Description

Lookup tables and some sequential logic functions composed the GLUE module.

Each LUT is composed by a 4-bit truth table and a decoder, allowing generation of any logic expression OUT as a function of two inputs. There is no direct output of OUT1 on I/O port. Only OUT0 is linked to I/O ports.

Figure 3-1. LUT Units Block Diagram

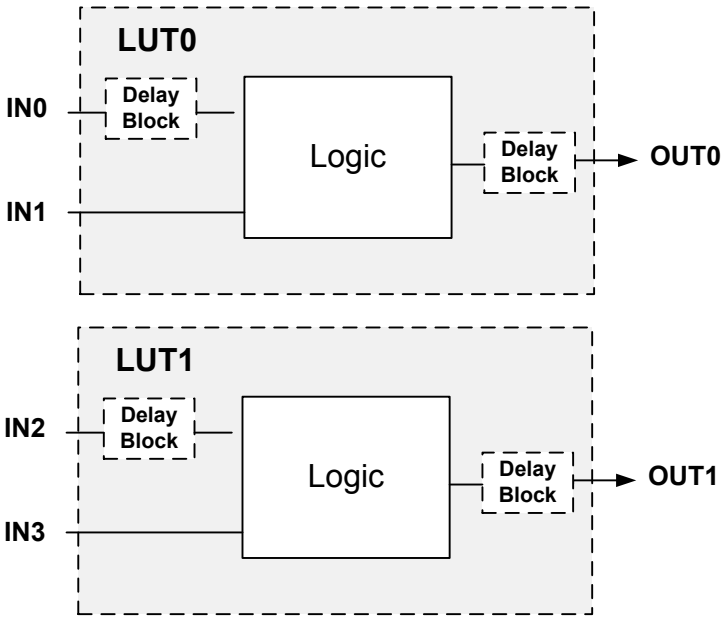


Figure 3-2. Truth Table for LUT0

IN1	IN0	OUT0
0	0	TRUTH0[0]
0	1	TRUTH0[1]
1	0	TRUTH0[2]
1	1	TRUTH0[3]

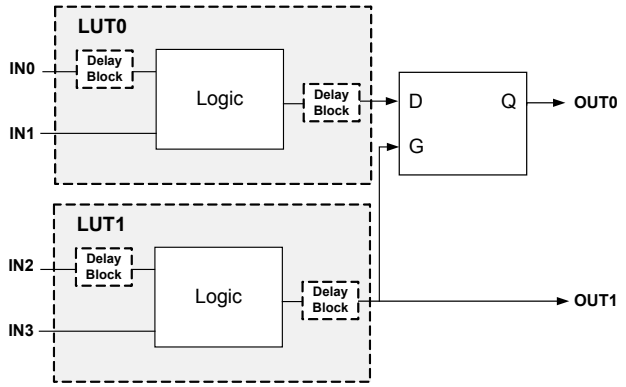
Figure 3-3. Truth Table for LUT1

IN3	IN2	OUT1
0	0	TRUTH1[0]
0	1	TRUTH1[1]
1	0	TRUTH1[2]
1	1	TRUTH1[3]

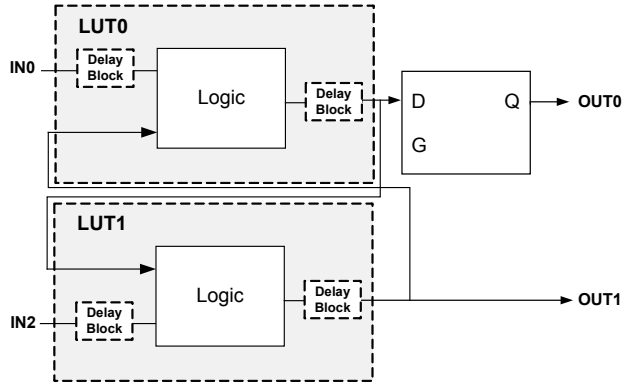
3.5 Sequential Logic Functions

Three sequential logic blocs are available: D Latch, D-Flip Flop, and RS Latch. LUTCONF[2:0] is used to select the sequential mode.

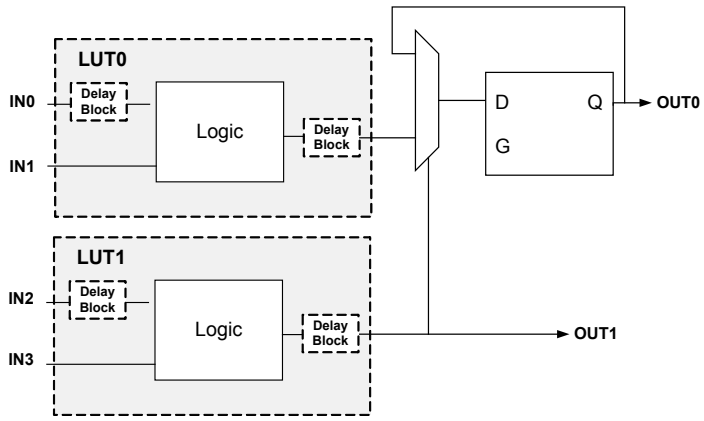
D-Latch: LUTCONF[2:0] = 101.



RS-Latch: LUTCONF[2:0] = 110.

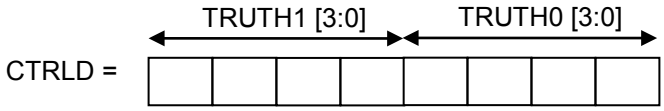


D-Flip-Flop: LUTCONF[2:0] = 111.



3.5.1 How to Program Logic Functions (AND, NAND, OR, NOR, XOR, XNOR, NOT)

1. **Select the logic function and program the CTRLD register:**



x = 0 for LUT0 x = 1 for LUT1	AND	NAND	OR	NOR	XOR	XNOR	NOT
THRUTHx[0]	0	1	0	1	0	1	1
THRUTHx[1]	0	1	1	0	1	0	X
THRUTHx[2]	0	1	1	0	1	0	X
THRUTHx[3]	1	0	1	0	0	1	0

2. **If a delay is needed, select the duration.**
Delay is not allowed on input and output together (not relevant).
DLYSEL field in CTRLC register selects a one cycle delay or a two cycle's delay.
The cycle corresponds to the peripheral clock period.

LUT0	LUT1	DLYSEL
1 cycle	1 cycle	00
2 cycles	1 cycle	01
1 cycle	2 cycles	10
2 cycles	2 cycles	11

3. **Select the location of the delay.**

	DLY0CONF
No delay	00
LUT0 input	01
LUT0 output	10

	DLY1CONF
No delay	00
LUT1 input	01
LUT1 output	10

4. **Select input pins and output pins for LUT0:**
Two ports are proposed for LUT0: PORTC or PORTD (see PORTSEL in CTRLA register).
Important remark: The port selected with PORTSEL is common for inputs and outputs.

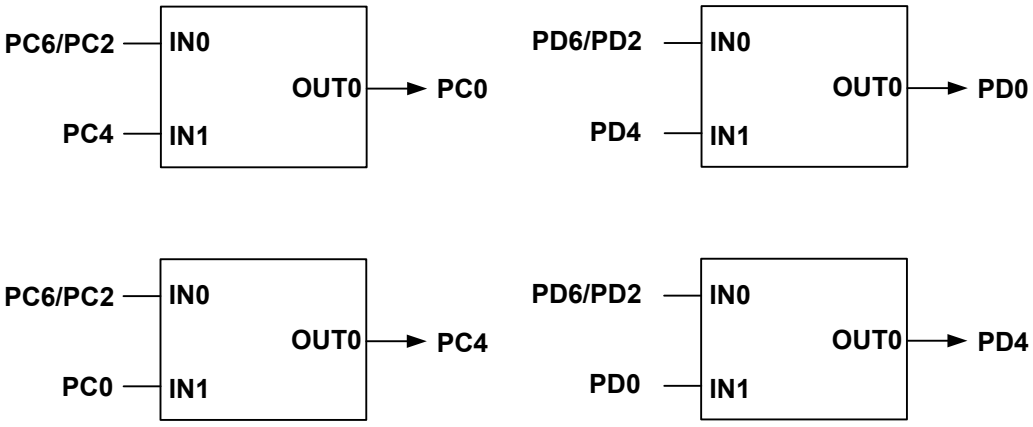
Pin selection for input and output is programmable using IN0SEL and LUT0OUTEN.

IN0SEL	IN0
11 (PINH)	PORTC6 or PORTD6
10 (PINL)	PORTC2 or PORTD2

IN1SEL	IN1
11 (PINH)	PORTC4 or PORTD4
10 (PINL)	PORTC0 or PORTD0

LUT0OUTEN	OUT0
01 (PIN0)	PORTC4 or PORTD4
10 (PIN4)	PORTC0 or PORTD0

Overview of allowed hardware configurations:



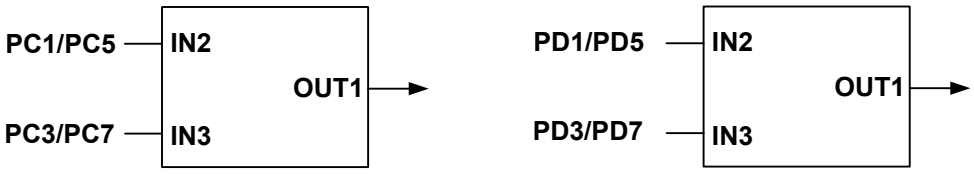
5. **Select input pins and output pins for LUT1:**
Two ports are proposed for LUT1: PORTC or PORTD (see PORTSEL in CTRLA register).
Important remark: This port is common for inputs and outputs and for LUT0 and LUT1.
Pin selection for input and output is programmable using IN1SEL and LUT1OUTEN.

IN1SEL	IN2
11 (PINH)	PORTC5 or PORTD5
10 (PINL)	PORTC1 or PORTD1

IN1SEL	IN3
11 (PINH)	PORTC7 or PORTD7
10 (PINL)	PORTC3 or PORTD3

LUT0OUTEN	OUT1
00	Event channel

Overview of allowed hardware configuration:



The LUT1 doesn't propose a direct connection on I/O pin (as LUT0). The LUT1 output on I/O is possible through the event system (see Section 3.5.2).

6. **Register configuration:**
To use LUT0 and LUT1 as separated LUT with two inputs and one output, the user has to program following registers:
   - PORTSEL to use PORTC or PORTD
   - LUT0OUTEN to select LUT0 output
   - 2LUT2IN in LUTCONF register

3.5.2 Event System on LUT1 Output

The XCL can generate an event by configuring the following registers:

- LUT0OUTEN (must be equal to 0x00, disable)
- CHxMUX to select XCL LUT0/1 output

The event system input comes from the XCL.

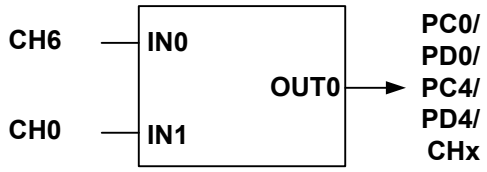
To output event on I/O pin (example on PORTA2):

Select CHx to output with ACEVOUT register.

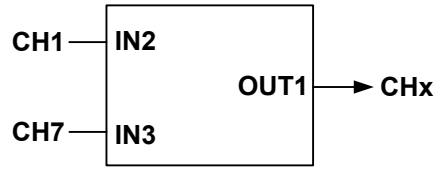
3.5.3 Event System as LUT Input

Event system is proposed as LUT input with selectable channels.

Programming IN0SEL[1:0] = 00 selects event system as source of LUT0 input:



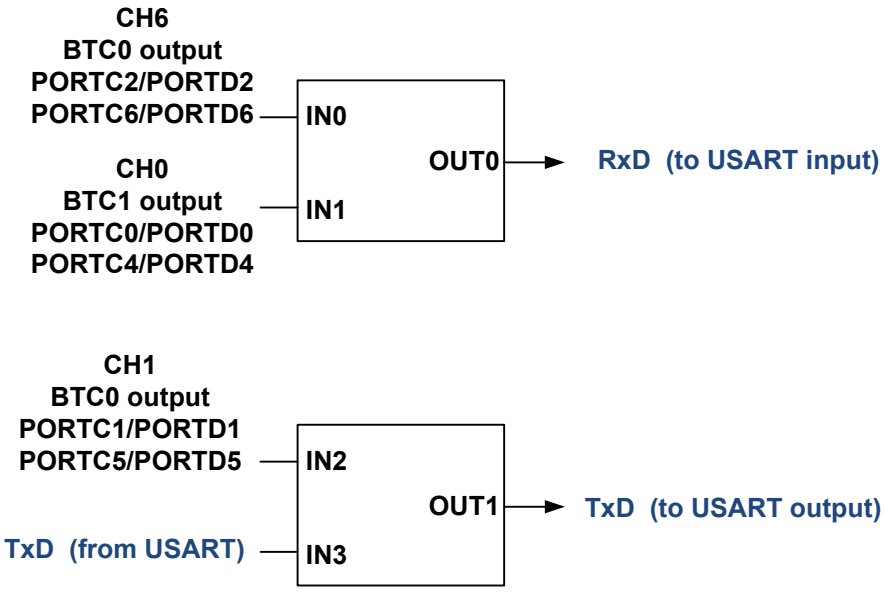
Programming IN1SEL[1:0] = 00 selects event system as source of LUT1 input:



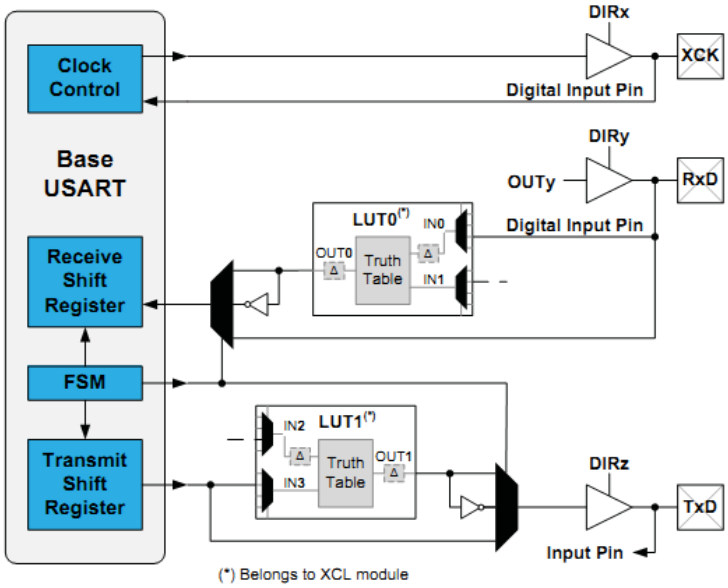
3.5.4 XCL as LUT Input

When XCL is selected as input in IN0SEL[1:0] or in IN1SEL [1:0], it corresponds to a connection of LUT input to USART or XCL Timer/Counters.

1. **XCL corresponds to USART:**
   LUT allows controlling USART signals as described below. LUT0 logical function is applied to USART RxD signal.
   LUT1 logical function is applied to USART TxD signal.



The CTRLD register from USART module must be programmed to enable USART and LUT connection.

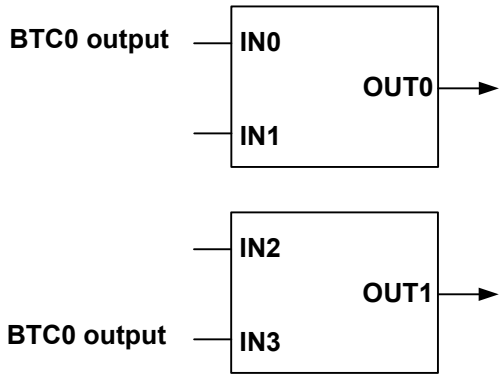


For the RxD control, the proposed inputs on IN0 and IN1 correspond to USART RxD input pins. The remapping of USART is also supported (example, from PC2 to PC6).

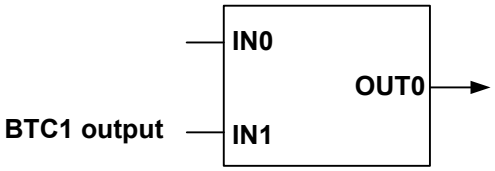
PORT C	Pin	TCC4	WEXC	TCC5	USARTC0	SPIC	TWI	XCL (LUT)	EXTCLK	AC OUT
PC0	16	OC4A	OC4ALS				SDA	IN1/OUT0		
PC1	15	OC4B	OC4AHS		XCK0		SCL	IN2		
PC2	14	OC4C	OC4BLS		RXD0			IN0		
PC3	13	OC4D	OC4BHS		TXD0			IN3		
PC4	12	OC4A	OC4CLS	OC5A		$\overline{SS}$		IN1/OUT0	EXTCLK	
PC5	11	OC4B	OC4CHS	OC5B	XCK0	SCK		IN2		
PC6	10	OC4C	OC4DLS		RXD0	MISO		IN0		AC1OUT
PC7	9	OC4D	OC4DHS		TXD0	MOSI		IN3		AC0OUT

PORT D	Pin	ADCAPOS GAINPOS	TCD5	USART D0	TWID (Bridge)	XCL (LUT)	XCL (TC)	CLOCK OUT	EVENT OUT	RTCOUT	ACOUT	REFD
PD0	28	ADC8			SDA	IN1/ OUT0						AREF
PD1	27	ADC9		XCK0	SCL	IN2						
PD2	26	ADC10		RXD0		IN0	OC0					
PD3	25	ADC11		TXD0		IN3	OC1					
PD4	24	ADC12	OC5A			IN1/ OUT0		CLKOUT	EVOUT			
PD5	23	ADC13	OC5B	XCK0		IN2						
PD6	22	ADC14		RXD0		IN0				RTCOUT	AC1OUT	
PD7	21	ADC15		TXD0		IN3		CLKOUT	EVOUT		AC0OUT	

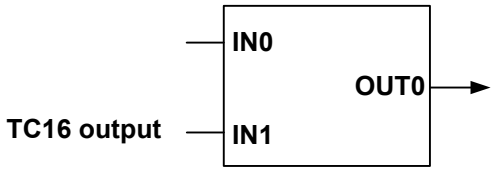
2. **XCL corresponds to XCL Timer/Counters:**
   BTC0, BTC1 and TC16 outputs can be connected to LUT inputs.
   If BTC0 is selected (BTC0, BTC01, BTC0PEC1, BTC0PEC2 modes), Timer output is available on IN0 and IN3 pins.



   If BTC1 is selected (BTC01, PEC0BTC modes), Timer output is available on IN1 pin.



   If TC16 mode is selected, Timer output is available on IN1 pin.



4. Timer/Counter Description

4.1 Overview

XCL includes two 8-bit timer/counters.

Each timer/counter supports normal, compare and input capture operation, with common flexible clock selections and event channels for each timer.

By cascading the two 8-bit timer/counters, the XCL proposes a 16-bit timer/counter.

USART can be connected to XCL to control the USART data length.

4.2 Features

XCL two independent 8-bit Timer/Counter has the following features:

- Period and compare channel for each Timer/Counter
- Input Capture for each timer
- Serial peripheral data length control for each timer (PEC mode)
- Timeout support for each timer
- Timer underflow interrupt/event
- Compare match or input capture interrupt/event for each timer

The 16-bit Timer/Counter (by cascading two 8-bit Timer/Counters) has the following features:

- Period and compare channel
- Input capture
- Timeout support
- Timer underflow interrupt/event
- Compare match or input capture interrupt/event

XCL timer/counter allows event time stamp, PWM generation, and frequency and period measurement.

4.3 Timer/Counter Definitions

Name	Description
PEC	8-bit peripheral counter. Can work only with the serial peripheral module
PEC2	8-bit peripheral counter is divided in two 4-bit peripheral counters
BOTTOM	The counter reaches BOTTOM when it becomes zero
MAX	The counter reaches maximum when it becomes all ones
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be equal to the period (PER) or the compare channel A (CCA) register setting. This is selected by the waveform generator mode
UPDATE	The Timer/Counter signals an update when it reaches BOTTOM or TOP, depending on the waveform generator mode
CLEAR	External peripheral, event system or CPU forces the (peripheral) Timer/Counter next value to BOTTOM
CC	Compare or capture

4.4 Description

Several configurations are available:

- Two 8-bit timer/counter (BTC0 and BTC1)
- One 16-bit timer/counter (TC16)
- One 8-bit timer/counter and one 8-bit peripheral counter (BTC0 + PEC1 or PEC0 + BTC1)
- Two 8-bit peripheral counters (PEC0 + PEC1)
- One 8-bit timer/counter and two 4-bit peripheral counters (BTC0 + PEC2)

Timer/Counters are decremented at each timer/counter clock input until CNT reaches BOTTOM (CNT = 0x00) and then reloads the counter with the Period Register value (CAPTPER).

4.5 Clock Sources

Timer/Counters can be clocked from:

- Pre-scaled peripheral clock (Timer mode)
- Event system (Counter mode)

At start-up and after reset, the default system clock is 2MHz (from internal 8MHz internal oscillator connected to a prescaler). This frequency corresponds to clkSYS.

The system clock is divided by prescalers A, B and C values to obtain clkPER. By default, clkSYS = clkPER.

4.5.1 Pre-scaled Peripheral Clock

The peripheral clock (clk_{PER}) is fed into a prescaler. The prescaler output is connected to BTC0 and BTC1 Timer/Counter inputs. CLKSEL [3:0] selects the pre-scaling (from 1to 1024). CLKSEL default values correspond to Timer/Counter in off state.

When TC16 configuration is programmed, the prescaler output is also connected to the TC16 input.

7	6	5	4	3	2	1	0
CMDSEL	TCSEL[2:0]			CLKSEL[3:0]			

CLKSEL[3:0]	Group configuration	Description
0000	OFF	None (i.e. Timer/Counter in OFF state)
0001	DIV1	Prescaler: clk_{PER}
0010	DIV2	Prescaler: $clk_{PER}/2$
0011	DIV4	Prescaler: $clk_{PER}/4$
0100	DIV8	Prescaler: $clk_{PER}/8$
0101	DIV64	Prescaler: $clk_{PER}/64$
0110	DIV256	Prescaler: $clk_{PER}/256$
0111	DIV1024	Prescaler: $clk_{PER}/1024$

4.5.2 Event System

Clock selection (CLKSEL) selects an event channel as the counter (CNT) input. Any event source, such as an external clock signal on any I/O pin, may be used as the clock input.

If an event channel is selected as counter input, CLKSEL is used to connect an event channel to Timer/Counter input.

7	6	5	4	3	2	1	0
CMDSEL	TCSEL[2:0]			CLKSEL[3:0]			

CLKSEL[3:0]	Group configuration	Description
1nnn	EVCHn	Event channel n (0 ≤ n ≤ 7)

In addition, the timer/counter can be controlled via the event system. The event selection (EVSRC) and event action (EVACT) settings are used to trigger an event action from one or more events.

7	6	5	4	3	2	1	0
EVACTEN	EVACT1[1:0]		EVACT0[1:0]		EVSRC[2:0]		

EVSRC[2:0]	Group configuration	Description
n	CHn	Event channel n

4.6 Interrupts

The XCL can generate both interrupts and events on:

- Timer/Counter underflow (BTC0 or BTC1)
- Compare or capture (BTC0 or BTC1)

Timer/counter events will be generated for all conditions that can generate interrupts.

The GLUE module generates only events.

INTCTRL[7:0] controls the interrupt system and INTFLAGS[7:0] contains the interrupt status. Depending on Timer/Counter configuration (TCSEL), fields in INTCTRL and INTFLAGS have different descriptions.

INTCTRL

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x07	TC16	INTCTRL	-	UNF0IE	-	CC0IE	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	BTC0	INTCTRL	-	UNF0IE	-	CC0IE	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	BTC01	INTCTRL	UNF1IE	UNF0IE	CC1IE	CC0IE	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	BTC0 PEC1	INTCTRL	PEC1IE	UNF0IE	-	CC0IE	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	PEC0 BTC1	INTCTRL	UNF1IE	PEC0IE	CC1IE	-	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	PEC01	INTCTRL	PEC1IE	PEC0IE	-	-	UNFINTLVL[1:0]		CCINTLVL[1:0]	
	BTC0 PEC2	INTCTRL	PEC2HIE	UNF0IE	PEC2LIE	CC0IE	UNFINTLVL[1:0]		CCINTLVL[1:0]	

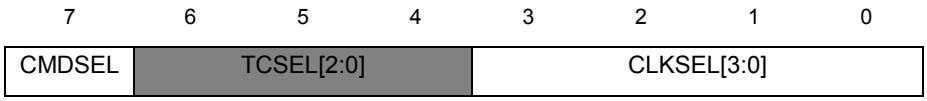
INTFLAG

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x08	TC16	INTFLAGS	-	UNF0IF	-	CC0IF (1)	-	-	-	-
	BTC0	INTFLAGS	-	UNF0IF	-	CC0IF (1)	-	-	-	-
	BTC01	INTFLAGS	UNF1IF	UNF0IF	CC1IF	CC0IF (1)	-	-	-	-
	BTC0 PEC1	INTFLAGS	PEC1IF	UNF0IF	-	CC0IF (1)	-	-	-	-
	PEC0 BTC1	INTFLAGS	UNF1IF	PEC0IF	CC1IF	-	-	-	-	-
	PEC01	INTFLAGS	PEC1IF	PEC0IF	-	-	-	-	-	-
	BTC0 PEC2	INTFLAGS	PEC2HIF	UNF0IF	PEC2LIF	CC0IF (1)	-	-	-	-

Note: 1. Not available in normal mode.

4.7 Timer/Counter Registers Description

The Timer/Counter configuration is controlled by TCSEL[2:0] in CTRLE.



The following table describes the different Timer/Counter modes.

TCSEL[2:0]	Configuration	Description
000	TC16	16-bit Timer/Counter with TC0 (LSB) and TC1(MSB)
001	BTC0	One 8-bit Timer/Counter (TC0)
010	BTC01	Two 8-bit Timer/Counters (TC0, TC1)
011	BTC0PEC1	One 8-bit Timer/Counter (TC0) and one 8-bit transmitter peripheral counter (PEC1)
100	PEC0BTC1	One 8-bit Timer/Counter with period (TC1) and one 8-bit receiver peripheral counter (PEC0)
101	PEC01	Two 8-bit transmitter /receiver peripheral counter (PEC0 and PEC1)
110	BTC0PEC2	One 8-bit Timer/Counter with period (TC0) and two 4-bit transmitter /receiver peripheral counter (PEC1 divided in two)
111	-	Reserved

Depending on this selection, register content is different for:

- INTCTRL, INTFLAGS (see Section 3.5)
- PLC/TEMP
- CNTL, CNTH
- CMPL, CMPLH
- PERCAPTL, PERCAPTH

0x09: TEMP/PLC

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x09	TC16	NORMAL	TEMP[7:0]							
		CAPTURE	TEMP[7:0]							
		PWM	TEMP[7:0]							
	BTC0	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC01	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0 PEC1	PERIPHERAL	PLC[7:0]							
		NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	PEC0 BTC1	PERIPHERAL	PLC[7:0]							
		NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	PEC01	PERIPHERAL	PLC[7:0]							
	BTC0 PEC2	PERIPHERAL	PLC[7:0]							
		NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-

0x0A: CNT/BCNT0/PCNT0

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0A	TC16	NORMAL	CNT[7:0]							
		CAPTURE	CNT[7:0]							
		PWM	CNT[7:0]							
	BTC0	NORMAL	BCNT0[7:0]							
		CAPTURE	BCNT0[7:0]							
		PWM	BCNT0[7:0]							
	BTC01	NORMAL	BCNT0[7:0]							
		CAPTURE	BCNT0[7:0]							
		PWM	BCNT0[7:0]							
	BTC0 PEC1	NORMAL	BCNT0[7:0]							
		CAPTURE	BCNT0[7:0]							
		PWM	BCNT0[7:0]							
	PEC0 BTC1	NORMAL	PCNT0[7:0]							
		CAPTURE	PCNT0[7:0]							
		PWM	PCNT0[7:0]							
	PEC01	PERIPHERAL	PCNT0[7:0]							
	BTC0 PEC2	NORMAL	BCNT0[7:0]							
		CAPTURE	BCNT0[7:0]							
		PWM	BCNT0[7:0]							

0x0B: CNT/BCNT1/PCNT1/PCNT1 + PCNT0

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0B	TC16	NORMAL	CNT[15:0]							
		CAPTURE	CNT[15:0]							
		PWM	CNT[15:0]							
	BTC0	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC01	NORMAL	BCNT1[7:0]							
		CAPTURE	BCNT1[7:0]							
		PWM	BCNT1[7:0]							
	BTC0 PEC1	NORMAL	BCNT1[7:0]							
		CAPTURE	BCNT1[7:0]							
		PWM	BCNT1[7:0]							
	PEC0 BTC1	NORMAL	BCNT1[7:0]							
		CAPTURE	BCNT1[7:0]							
		PWM	BCNT1[7:0]							
	PEC01	PERIPHERAL	BCNT1[7:0]							
	BTC0 PEC2	NORMAL	PCNT1[3:0]				PCNT0[3:0]			
		CAPTURE	PCNT1[3:0]				PCNT0[3:0]			
		PWM	PCNT1[3:0]				PCNT0[3:0]			

0x0C: Unused

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0C	TC16	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC01	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0 PEC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	PEC0 BTC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0 PEC2	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-

0x0D: Unused

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0D	TC16	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC01	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0 PEC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	PEC0 BTC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-
	BTC0 PEC2	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	-	-	-	-	-	-	-	-

0x0E: PER/CAPT/CMP/PER0/CAPT0/BPER0/BCAPT0/BCMP0/BCMP1

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0E	TC16	NORMAL	PER[7:0]							
		CAPTURE	CAPT[7:0]							
		PWM	CMP[7:0]							
	BTC0	NORMAL	PER0[7:0]							
		CAPTURE	CAPT0[7:0]							
		PWM	BPER0[7:0]							
	BTC01	NORMAL	BPER0[7:0]							
		CAPTURE	BCAPT0[7:0]							
		PWM	BCMP0[7:0]							
	BTC0 PEC1	NORMAL	BPER0[7:0]							
		CAPTURE	BCAPT0[7:0]							
		PWM	BPER0[7:0]							
	PEC0 BTC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	BCMP1[7:0]							
	BTC0 PEC2	NORMAL	BPER0[7:0]							
		CAPTURE	BCAPT0[7:0]							
		PWM	BPER0[7:0]							

0x0F: PER/CAPT/CMP/CMP0/BPER1/BCAPT1/BCMP1/BCMP0

Address	Selection	Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x0F	TC16	NORMAL	PER[15:8]							
		CAPTURE	CAPT[15:8]							
		PWM	CMP[15:8]							
	BTC0	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	CMP0[7:0]							
	BTC01	NORMAL	BPER1[7:0]							
		CAPTURE	BCAPT1[7:0]							
		PWM	BCMP1[7:0]							
	BTC0 PEC1	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	BCMP0[7:0]							
	PEC0 BTC1	NORMAL	BPER1[7:0]							
		CAPTURE	BCAPT1[7:0]							
		PWM	BPER1[7:0]							
	BTC0 PEC2	NORMAL	-	-	-	-	-	-	-	-
		CAPTURE	-	-	-	-	-	-	-	-
		PWM	BCMP0[7:0]							

4.8 Timer/Counter Operation Selection

Timer/Counter operation mode is selected with MODE[1:0] bits in CTRLF register.

7	6	5	4	3	2	1	0
CMDEN[1:0]		CMP1	CMP0	CCEN1	CCEN0	MODE[1:0]	

MODE[1:0]	Group configuration	Description
00	NORMAL	Normal mode, with period
01	CAPT	Capture mode
10	PWM	Single-slope PWM
11	1SHOT	One-shot PWM

List of the proposed operation mode according to mode selection.

	Normal	Capture	PWM	1 shot PWM
TC16	X	X	X	X
BTC	X	X	X	X
PEC	X	X		

4.8.1 Normal Operation

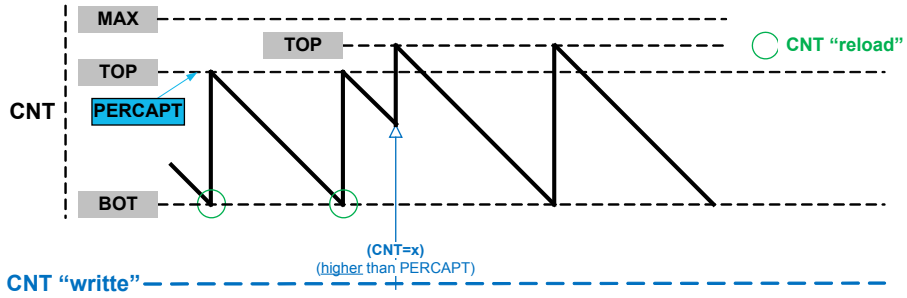
The Timer/Counter decrements CNT register from TOP to BOTTOM:

TOP stored in PLCL register.

BOTTOM corresponds to 0x00 in CNTL register.

If TC16 mode is selected, PLCH and CNTH are added to support MSB.

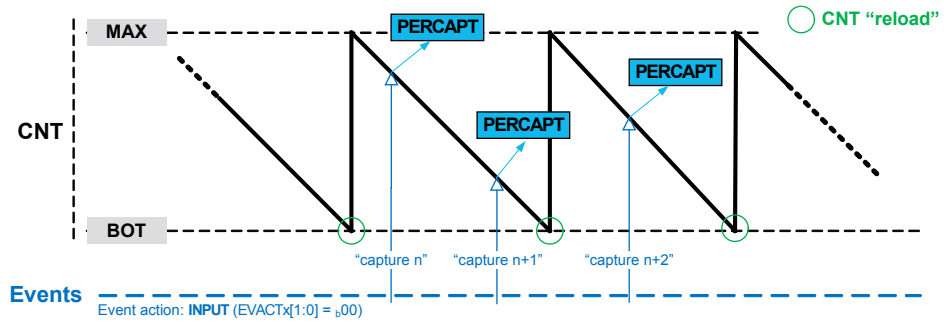
The CNT reload is automatic when Timer/Counter reaches the BOTTOM value.



4.8.2 Capture Operation

Capture input in linked to event system. The counter counts down from MAX to BOTTOM and stored CNT value in PERCAPT when an event appears.

MAX is stored in PLCL register.



Several capture modes are selectable:

- Event input: When the event appears, capture action is started
- Frequency capture: Only the rising edge of the signal to measure triggers the capture operation
- Pulse width capture: The rising edge and the falling edge of the signal to measure trigger the capture operation

7	6	5	4	3	2	1	0
EVACTEN	EVACT1[1:0]		EVACT0[1:0]		EVSRC[2:0]		

CLKSEL[1:0]	Group configuration	Description
00	INPUT	Input capture
01	FREQ	Frequency capture
10	PW	Pulse width capture
11	RESTART	Restart CNT

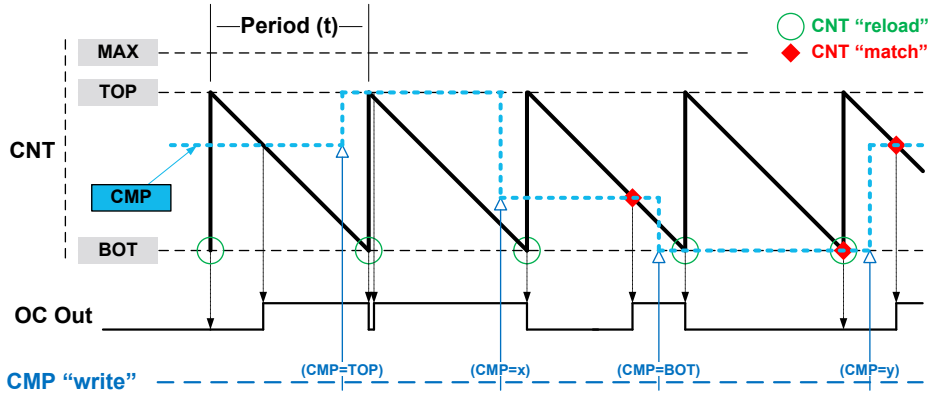
4.8.3 PWM Generation

This mode corresponds to the single slope PWM mode.

The Timer/Counter counts from TOP to BOTTOM. When CNT reaches the CMP value, the OC output triggers.

TOP is stored in CMP register. OC frequency depends on TOP value and XCL clock.

Pulse width depends on CMP value (inversely proportional).



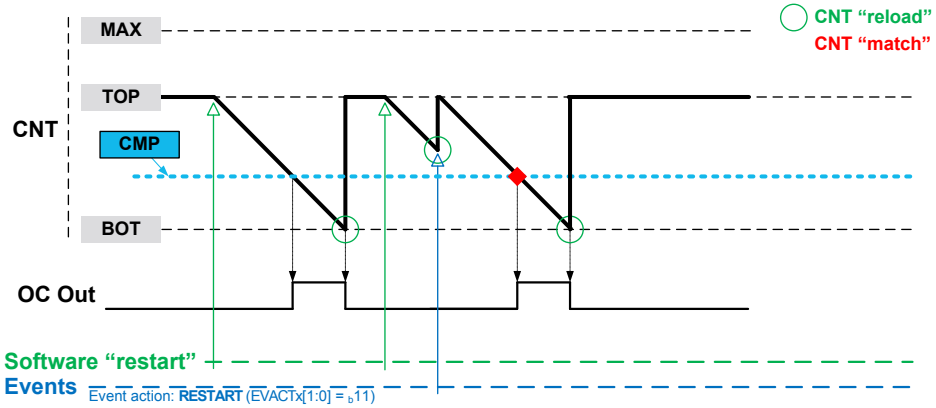
4.8.4 Single Shot PWM Mode

In single shot mode, the start and stop Timer/Counter operations are controlled by external event or software commands.

Start timer operation is performed with CMDSEL.

7	6	5	4	3	2	1	0
CMDSEL	TCSEL[2:0]			CLKSEL[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CMDSEL	Group configuration	Description
0	NONE	None
1	RESTART	Force Restart CNT



4.9 Output Compare

On the Atmel XMEGA E family, PORTC and PORTD are available for OC. The alternate function section of the datasheet gives the OC pinout (XCL-TC column).

PORT C	PORT D	XCL-LUT	XCL-TC
PC0	PD0	IN1/OUT0	
PC1	PD1	IN3	
PC2	PD2	IN0	
PC3	PD3	IN2	
PC4	PD4	IN1/OUT0	
PC5	PD5	IN3	
PC6	PD6	IN0	CC0
PC7	PD7	IN2	CC1

PORTSEL selects the PORT used for OC output. This port selection is common for LUT/USART/OC.

Bit	7	6	5	4	3	2	1	0
+0x00	LUT0OUTEN[1:0]		PORTSEL[1:0]		-	LUTCONF[2:0]		

PORTSEL[2:0]	Group configuration	Description
00	PC	Port C
01	PD	Port D

4.10 16-bit Timer/Counter

The BTC0 and BTC1 are two 8-bit Timers/Counters. When BTC0 and BTC1 are cascaded, it creates a truth 16-bit Timer/Counter (TC16) with 16-bit period, compare and capture registers.

The 16-bit Timer/Counter input clock is controlled by TCSEL.

4.11 Peripheral Counter Operation (PEC)

When USART is used with XCL, the data length of the frame can be controlled by the peripheral counter. This mode is used to send or receive variable frame length up to 255.

The XCL interacts with USART. The USART can be set in SPI mode and used for SPI communication. The SPI data length frame can be controlled by PEC.

If Rx and Tx signals are connected to LUT, signals are encoded/decoded before processing.

4.12 PEC2: Two 4-bit Peripheral Counter

This mode provides two peripheral counters (PEC2H and PEC2L) with using only one 8-bit counter (BTC1).

XCL proposes up to 15 data bits for UART but on two Tx/Rx lines.

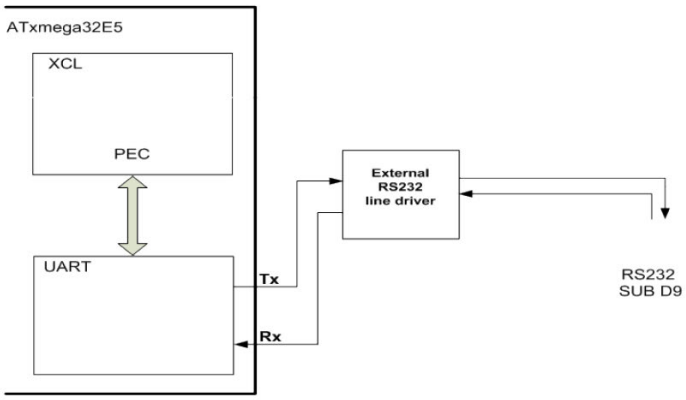
The only mode available with PEC2 is when TCSEL [2:0] = 110.

It corresponds to BTC0PEC2:

- BTC0 (8-bit timer/counter TC0)
- PEC2 (4-bit peripheral counter PEC2H and PEC2L based on BTC1)

5. Example of XCL Application: Variable Frame Length

This application example is a 12-bit UART with asynchronous serial receiver and transmitter: PEC is used to control the transmitter frame data length.



5.1 Frame Format

Data transfer is frame based. A serial frame consists of one character of data bits with synchronization bits (start and stop bits) and an optional parity bit for error checking.

UART proposes only 5, 6, 7, or 9 data bits.

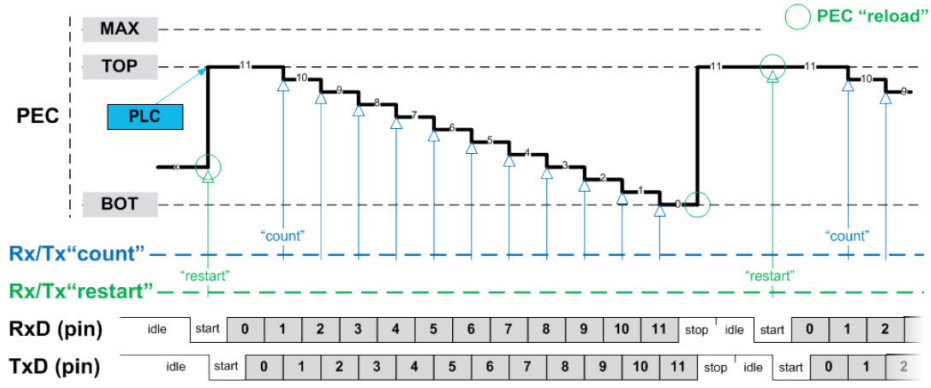
XCL proposes up to 255 data bits.

Before enabling the transmitter, XCL must be configured:

- Pre scaled peripheral clock (to fit with UART baud rate)
- PORTSEL[1:0] to select USARTC0 or USARTD0 for PEC
- Data length in PLC register: PLC = data length – 1
- TCSEL[2:0] for PEC selection

A transmission is initiated by loading the transmit buffer (DATA) with the data to be sent. When the first data is loaded in the shift register, the USART provides the restart command to the peripheral counter.

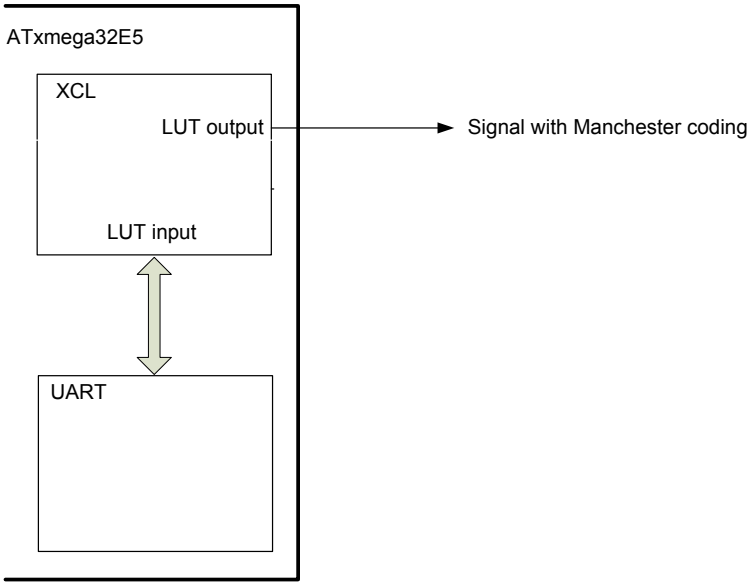
Each bit shift will decrement the peripheral counter. A compare match is provided by the XCL when the internal counter value reaches BOTTOM (zero). While the compare match is not received, the USART continues to shift out the data bits.



6. Example of XCL Application: Signal Encoding

This application example is a Manchester coding of a signal from the UART:

- LUT is used to process output signal



6.1 UART Configuration:

CTRLD register controls the connection between the UART and the XCL. This register allows configuring:

- DECTYPE: these bits decide the decoding encoding type applied to receiver and transmitter
- LUTAC: these bits decide the action the UART performs when linked to LUT
- PECACT: these bits decide the PEC action to perform

UART CTRLD

Bit	7	6	5	4	3	2	1	0
+0x05	-	-	DECTYPE[1:0]		LUTACT[1:0]		PECACT[1:0]	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DECTYPE[1:0]	Group configuration	Description
00	DATA	LUT OUT applies during data field only
01	SDATAS	LUT OUT applies during start, data and stop fields
10	SDATA	LUT OUT applies during start and data field
11	NOTSDATA	- Inverted LUT OUT applies during start field - LUT OUT applies during data field

LUTACT[1:0]	Group configuration	Event action
00	OFF	Standard Configuration
01	RX	Enable decoding for on receiver engine
10	TX	Enable encoding on transmitter engine
11	BOTH	Enable both encoding/decoding

PECACT[1:0]	Group configuration	Event action
00	OFF	Standard Configuration
01	PEC0	Receiver data length controlled by peripheral counter 0
10	PEC1	Transmitter data length controlled by peripheral counter 1
11	PEC01	- Receiver data length controlled by peripheral counter 0 - Transmitter data length controlled by peripheral counter 1

6.2 LUT Configuration:

Before enabling the UART transmitter, XCL must be configured:

- LUT input and LUT output
- LUTCONF[2:0] for LUT configuration
- INxSEL[1:0] to select XCL as LUT input
- TRUTHx[3:0] for truth table definition for LUT
- TCSEL[2:0] for PEC selection

7. ASF (Atmel Software Framework) Examples

The ASF proposes several software examples. Project with C source code is available. Access to examples is possible using the Atmel Studio 6 and File/New/Example Project from ASF.

The number of ASF examples for XCL is currently four.

7.1 XCL Example 1 – STK600 - ATxmega32E5

This example configures XCL LUT0 sub-module to perform a logic XOR operation between its two inputs pins IN0/IN1 map on the low nibble of PORTD (respectively PD2, PD0). The LUTO output pin is mapped to PORTD pin 4. As this XCL configuration is purely asynchronous, the example enters Power Down sleep mode, but the XOR operation between the two pins is still functional.

http://asf.atmel.com/docs/3.5.0/xmega.drivers.xcl.example1.stk600-rc032x_atxmega32e5/html/index.html

7.2 XCL Example 2 – STK600 - ATxmega32E5

This example will configure the XCL Timer sub-module in a 16-bit timer with its underflow interrupt to toggling an LED at 4Hz.

http://asf.atmel.com/docs/3.5.0/xmega.drivers.xcl.example2.stk600-rc032x_atxmega32e5/html/index.html

7.3 XCL Example 3 – STK600 - ATxmega32E5

This example demonstrates how to use both Timer and LUT sub-modules together within the XCL module. The purpose of this configuration is to generate a waveform output that is the logic XOR of two generated PWM waveforms. This example configures XCL TC sub-module in two 8bits BTCO/1 timers to generate single slope PWM output on their compare output pins (PD2 and PD3). Those PWM outputs are internally connected to LUT0/1 inputs configured as logic XOR function. The resulting waveform is connected to PD4 LUT output.

http://asf.atmel.com/docs/3.5.0/xmega.drivers.xcl.example3.stk600-rc032x_atxmega32e5/html/index.html

7.4 XCL Example 4 – STK600 - ATxmega32E5

This example configures XCL LUT sub-module LUT0/LUT1 in one 3-inputs LUT to perform a logic XOR operation between the three external inputs pins IN0/IN2/IN3 map on the low nibble of PORTD (respectively PD2, PD1 and PD3). The LUTO output pin is mapped to PORTD pin4. As this XCL configuration is purely asynchronous, the example enters Power Down sleep mode, but the XOR operation between the three pins is still functional.

http://asf.atmel.com/docs/3.5.0/xmega.drivers.xcl.example4.stk600-rc032x_atxmega32e5/html/index.html

8. Revision History

Doc. Rev.	Date	Comments
42083B	09/2014	§3.5.1: The table in “1. Select the logic function and program the CTRLD register” has been corrected for XOR and XNOR
42083A	04/2013	Initial document release

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