Description

This FAQ answers frequently asked questions concerning ATR2406 and its use.
1. Transmitter

1.1 T-Q1: Which Data Rates are Supported by ATR2406?
T-A1: The ATR2406’s supported data rates are 72Kbps, 144Kbps, 288Kbps, 576Kbps and 1152Kbps.

1.2 T-Q2: Is it Possible to Use Asynchronous Data Alongside Synchronous Data? Does the TX_DATA Have to be in a Special Relationship to the Reference Clock?
T-A2: TX_DATA has to be in sync with the reference clock with fast TX_DATA (1152Kbps).
At lower data rates, there is no requirement for this, as the artificial jitter caused by not being in synchronisation is small compared to the bit-width.
The reason is that the internal Gaussian filter circuit oversamples the transmit data at time points which are referenced by the REF_CLK.
The oversampling is carried out 6 times per bit.
So if the transmit data is not synchronised, and, for example, a “101010” pattern is not sampled correctly (say the “1” is sampled just 4 times, than the following “0” is sampled 8 times, etc.) the Gaussian filtering will not work properly.
With synchronised transmit data, the oversampling will always carried out correctly

1.3 T-Q3: What is the Maximum Possible Slot Length?
T-A3: As a rule of thumb, the maximum slot length will be longer if the loop filter has bigger capacitor values. However, the settling time for the PLL will also be increased by using a bigger capacitor, which implies a bigger loop filter time constant.
For details please see the application note “ATR2406 Loop Filter and Data Rates”.

1.4 T-Q4: What is the Reason for Frequency Drift on Open-loop Systems?
Frequency drift is an issue which applies to all systems using open-loop mode.
The maximum possible slot length depends on the frequency drift at open-loop enable.
The frequency drift is determined by the leakages of the external loop filter components, the leakage currents via the PCB and the leakage of the VTUNE input of ATR2406 which together cause a slowly drifting frequency when the PLL is in open-loop mode.
For tips on reducing the drift and optimizing it for the application requirements please see the application note “ATR2406 Loop Filter and Data Rates”.

2. Receiver

2.1 R-Q1: The Datasheet States that Clock Recovery is only Available when the Data Rate is Set to 1152Kbps. Does the Clock Recovery Function Work at Data Rates other than 1152Kbps?

R-A1: Yes and no.

It is true that clock recovery is designed to work at 1152Kbps. For example, if you have a “101010” pattern, the clock recovery will mark the middle of the bit position where the microcontroller can sample the data.

However, if you have a “110011” you will get two marks at the 1s and two marks at the 0s; also, a “11001100” pattern can be the preamble of a 576Kbps bitstream.

So, it is possible to use clock recovery at lower bitrates (integer dividers of 1152Kbps) by blanking out the double-marks per bit using software. Figure 2-1 illustrates this issue.

Figure 2-1. Recovered Clock Versus Received Bits and Different Data Rates

2.2 R-Q2: So, in the Case of Lower Data Rates, the Microcontroller Will Need to Oversample the Data or Use Other Sampling Techniques to Decode the Incoming Bit Stream?

R-A2: The clock recovery function is very useful at high data rates to reduce the MCU load. At data rates below 1152Kbps it might be more convenient for an MCU to oversample or poll the incoming data, than to use the clock recovery function.

2.3 R-Q3: What is the Bandwidth of the RX Section?

R-A3: The bandwidth of the RX section is defined by the internal filter, which is 1450kHz.

2.4 R-Q4: What is the Maximum Duration for a “1” or “0” before Dataslicer Threshold Point Drifts Away?

R-A4: One strength and big advantage of our ATR2406 compared to competing products is that there is no analog dataslicer inside, it is a purely digital demodulator.

So, there is no drift nor are there restrictions on sync word length and data message in real applications. The maximum transmit slot length is determined by the loop filter time constant. For more details please see the application note “ATR2406 Loop Filter and Data Rates”.

Figure 2-1. Recovered Clock Versus Received Bits and Different Data Rates
2.5 **R-Q5: Are there any Restrictions on Preamble Length, Sync Word Length or on Data Message Length?**

R-A5: Since ATR2406 uses a digital demodulator there are no restrictions on lengths of sync word or data message. However, the preamble length should be $\geq 16$ bits.

2.6 **R-Q6: Does that Imply that the RX Clock Provided by the Device Does not Depend on any Particular Number of Preamble Bits before it Provides an Accurate Strobe or Clock Signal Allowing the Attached Microcontroller to Properly Sample the RX Data?**

R-A6: The function of the digital demodulator can be roughly seen as follows:

- Internally, there is a frequency detector to decide if the incoming data is a "0" or a "1".
- This detector also includes an internal oscillator which is synchronised by the preamble, so a preamble is required to obtain synchronization.
- The RX data and the RX clock are recovered from the received signal.
- Therefore, the minimum preamble should be at least 16 bits (about 16$\mu$s).
3. General

3.1 G-Q2: Can I Use a Low-cost Crystal?
G-A2: The tolerance of the crystal should be less than or equal to ±20ppm.

Background: A crystal frequency which is, for example, only +20ppm higher than the specified center frequency will lead to a frequency offset of about 50kHz at 2.45GHz. Taking this into calculation, a “±” tolerance will cause a worst-case separation of 100kHz. Since ATR2406 utilizes a high deviation of 400 kHz, and the internal automatic adjustment circuit covers slightly more than this, the worst-case offset can be accepted without impacting performance.

3.2 G-Q3: Is a Layout for an RF Demo Board Available?
Yes. You can download the actual layout, including gerber files, substrate data, bill of materials and module description from our website: http://www.atmel.com/products/smartrf/

3.3 G-Q3: How Can the Power Consumption be Reduced?
G-A3: The power consumption can be reduced by using burst mode.

A data packet has to be sent as fast as possible to keep on-the-air time (OTA) as low as possible. By using small transmit and receive bursts, the average power consumption is reduced significantly.

3.4 G-Q4: Which Kind of Substrate are you Using on your RF Demo Board?
G-A4: The substrate we are using on our RF demo board is standard FR4 (eps_r ~ 4.4) – two layers.
The substrate height is 500µm and the conductor thickness (copper) is 35µm.
All structures (track width, microstrip, etc.) are implemented in such a way that standard tolerances do not affect the performance of the RF demo board at all.
Beyond this, other substrate thicknesses are possible (for example, 800µm, 1000µm); however, the microstrip elements have to be adapted to this height.

3.5 G-Q5: What Loop Filter Components Should be Used?
G-A5: To obtain best dynamic performance and low frequency drift, use high-quality external loop filter capacitors. COG-type capacitors have low leakage as well as low dielectric absorption, both of which are important parameters on systems using open-loop modulation.
For more details, please see the application note “ATR2406 Loop Filter and Data Rates”.

3.6 G-Q6: How Can I Interface the ATR2406 to an AVR Microcontroller?
G-A6: This following describes how an AVR microcontroller can be connected to the ATR2406. The main focus is on the exchange of RF data (how the data to be transmitted can be sent from the AVR to the ATR2406, and how the data received can be brought from the ATR2406 to the AVR microcontroller).

3.6.1 Interfacing the AVR with the ATR2406 via Synchronous UART
This is the method used by our RF firmware. This interfacing method is a very effective way of connecting the AVR and the ATR2406 together. To get such a system working, the user has to configure the maximum data rate of the ATR2406 and enable the clock recovery feature. The maximum data rate is only available when using the UART in synchronous mode.

3.6.1.1 Configuration of the ATR2406
- Enable the clock recovery feature for receiving of RF data
- Disable the clock recovery feature for transmitting of RF data
3.6.1.2 Configuration of the AVR UART

- Configure the UART in synchronous mode (set UMSEL bit in the UCSRC register)
- Set the baudrate register to 1152Kbps

Figure 3-1. Principal Interconnection Between AVR and ATR2406

Figure 3-2. Improved Interconnection between AVR and ATR2406
3.6.2 Interfacing the AVR with the ATR2406 via Asynchronous UART

This method of interfacing the AVR with the ATR2406 enables the user to get all the possible data rates other than 1152Kbps.

3.6.2.1 Configuration of the ATR2406

- Disable the clock recovery feature for data transmission and reception

3.6.2.2 Configuration of the AVR UART

- Configure the UART in asynchronous mode (clear the UMSEL bit in the UCSRC register)
  - Set baudrate register to 576Kbps, 288Kbps, 144Kbps, or 72Kbps

  → One big advantage of using the UART: Synchronisation to the incoming RF data stream is done automatically by hardware.

3.6.3 Interfacing the AVR with the ATR2406 via SPI

This is a second possibility of interfacing the two chips, however, it is a very complex one as the CPU load is heavily increased. First, the SCK has to be generated by software as the hardware does not support one of the possible data rates. Second, the synchronization to the incoming RF data stream must also be handled by software.

3.6.4 Interfacing the AVR with the ATR2406 via Software

To do this, the software has to handle all steps necessary to receive or transmit data via RF. This method is possible at lower data rates but adds a big overhead to the software.

3.7 G-Q7 How Can I Use the ATR2406 without an AUX-regulator Transistor?

G-A7: When using the ATR2406 without the AUX regulator, the maximum allowed supply voltage is 2.9V to 3.6V, and the pins VREG, VS_REG, VS_IFD, VS_IFA, VS_SYN, VS_TRX need to be connected directly to this supply voltage.

REG_CTRL must to connected to the supply voltage via a resistor (for example, 10kΩ).

PU_REG can be connected together with PU_TRX and controlled via one control signal by the MCU.

3.8 G-Q8 Can I Increase the Settling Time of the PLL?

G-A8: Yes. For details, see the application note “ATR2406 Loop Filter and Data Rates”.

3.9 G-Q9 What are the Requirements for the PCB and Microstrip Lines of the RF Module?

G-A9: All mechanical dimensions and specifications of the used substrate and microstrip lines can be provided upon request.

3.10 G-Q10: Why do You Use Two Capacitors in Parallel (C18 = 470 nF, C19 = 68 pF) at the VCO Regulator (pin 13 of ATR2406) Instead of only one 470 nF, which is the Dominant Value?

G-A10: The reason for having two caps at this point, one with high capacitance and one with low capacitance (both have different ESRs and resonant frequencies), is to obtain a wideband filtering characteristic. The cap with 68pF corresponds to any noise which has higher frequency components improving the filtering at the VCO regulator pin of ATR2406. So this will reduce any noise which might be coupled in on the VCO regulator.
4. **Revision History**

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>History</th>
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