



High-speed, Loadable 16-bit Binary Counter

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a fast synchronous, loadable 16-bit binary counter that operates at 70 MHz on and off chip under the worst commercial operating conditions. The use of prescaled logic to generate the carry-enable signals for each count bit allows faster operation than traditional carry-enable generation methods. The 16-bit counter is very compact, yet the inputs and outputs are readily accessible.

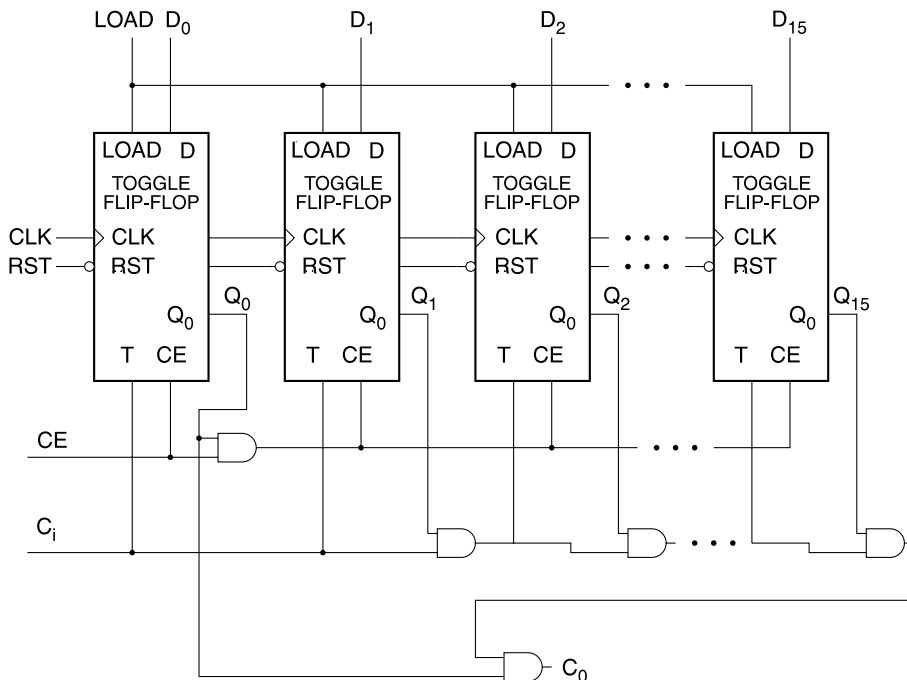
Description

Figure 1 shows a block diagram representation of the counter architecture and I/O. CLK is the clock signal, RST is the reset signal, and LOAD is the load data signal. CE is the count enable signal. CLK is a positive, edge-triggered synchronous signal, RST is an active low, asynchronous signal, and LOAD is an active low, synchronous signal. Pins D_0 through D_{15} are the load data inputs, pins Q_0 through Q_{15} are the count bits. Pin C_i is the carry in, C_o is the carry out. Toggle flip-flops are used as the register elements for each bit of the counter. They toggle on the rising edge of CLK when their RST, CE, and T inputs pins are high and the LOAD pin is low.

Field Programmable Gate Array

Application Note

Figure 1. Architecture and I/O of 16-bit Counter



Initial power-up of the AT6000 device resets all the registers so the counter begins counting on the first rising edge of CLK if C_i , RST, and CE are set high and LOAD is set low. The circuit counts by allowing each register element to toggle in succession on the rising edge of CLK if the Q outputs of all prior elements are asserted.

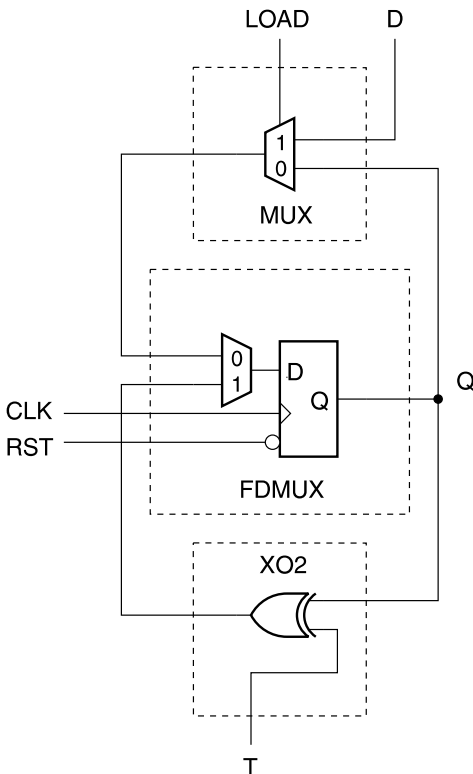
Asserting RST at any time inhibits counting, but also resets the registers to low values.

Figure 2 shows the implementation of a register element in the 16-bit counter logic architecture. The Q output of this circuit will toggle if T and CE are high and LOAD is low on the rising edge of CLK. If CE and LOAD are low, then Q will not change, regardless of T. If CE is high and LOAD is low, then Q will remain the same if T is low upon the rising edge of CLK.

To load a value into the counter, LOAD is set high and CE is set low before the rising edge of CLK. The value is latched into the register elements on the rising edge of CLK.

CE should then be held low until after the next rising edge of CLK to allow the carry-enable logic time to recalculate the T inputs for each register element. The carry-enable logic is the chain of two-input AND gates that generates the T signal inputs.

Figure 2. Schematic of 16-bit Counter Register Element



If LOAD is asserted for one clock cycle and CE is low for two clock cycles, the data at D_{0-15} is loaded into the registers on the first clock cycle, and the counting continues from the newly loaded value on the second cycle (Figure 3).

During the LOAD cycle, when the data at D_{0-15} is clocked into the counter, the carry-enable logic must have time to generate and propagate the results to every bit. Since an arbitrary number at D_{0-15} can cause a carry-enable signal to propagate along the entire length of the carry-enable chain, the critical path during a LOAD operation has the potential to pass through 14 AND-gate (AN2) stages before entering the last register element. By holding the CE signal low an extra clock cycle to inhibit the counting operation (as shown in Figure 3), the carry-enable logic has additional time to propagate the correct values to each bit.

During normal operation Q_0 , the least-significant bit of the counter, is also a fast carry-enable signal. As shown in Figure 4, the CE inputs of each register element ahead of the first bit are tied to the Q_0 . All bits greater than Q_0 must wait for Q_0 to switch from low to high before they can change on the rising edge of CLK. As the more significant bits change, their values trickle forward through the two-input AND gates that form the carry-enable logic to the T inputs of succeeding register elements. Distributing Q_0 in this manner allows an extra clock cycle for the chain of two-input AND gates to calculate the carry-enable signal for the T input of each register element.

The exact layout of the fast carry-enable logic for the first several bits of the 16-bit counter is shown in Figure 5. By replicating and concatenating the circuitry surrounded by the dotted box, the entire counter function is realized. The AN2 gates feed two-input XOR gates, (XO2). The FDMUX macro provides a two-to-one multiplexer feeding the input of a D-type flip-flop in a single cell. The MUX macro is a one-cell two-to-one multiplexer.

The performance and utilization statistics are given in Table 1. Both implementations are available in schematic and layout form.

Figure 3. Timing Diagram of Counter Load Cycle

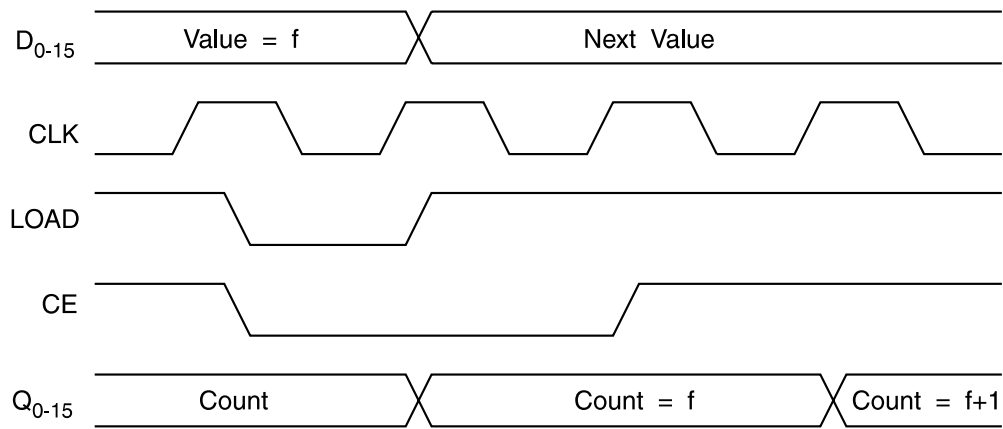


Figure 4. Schematic of Counter Architecture

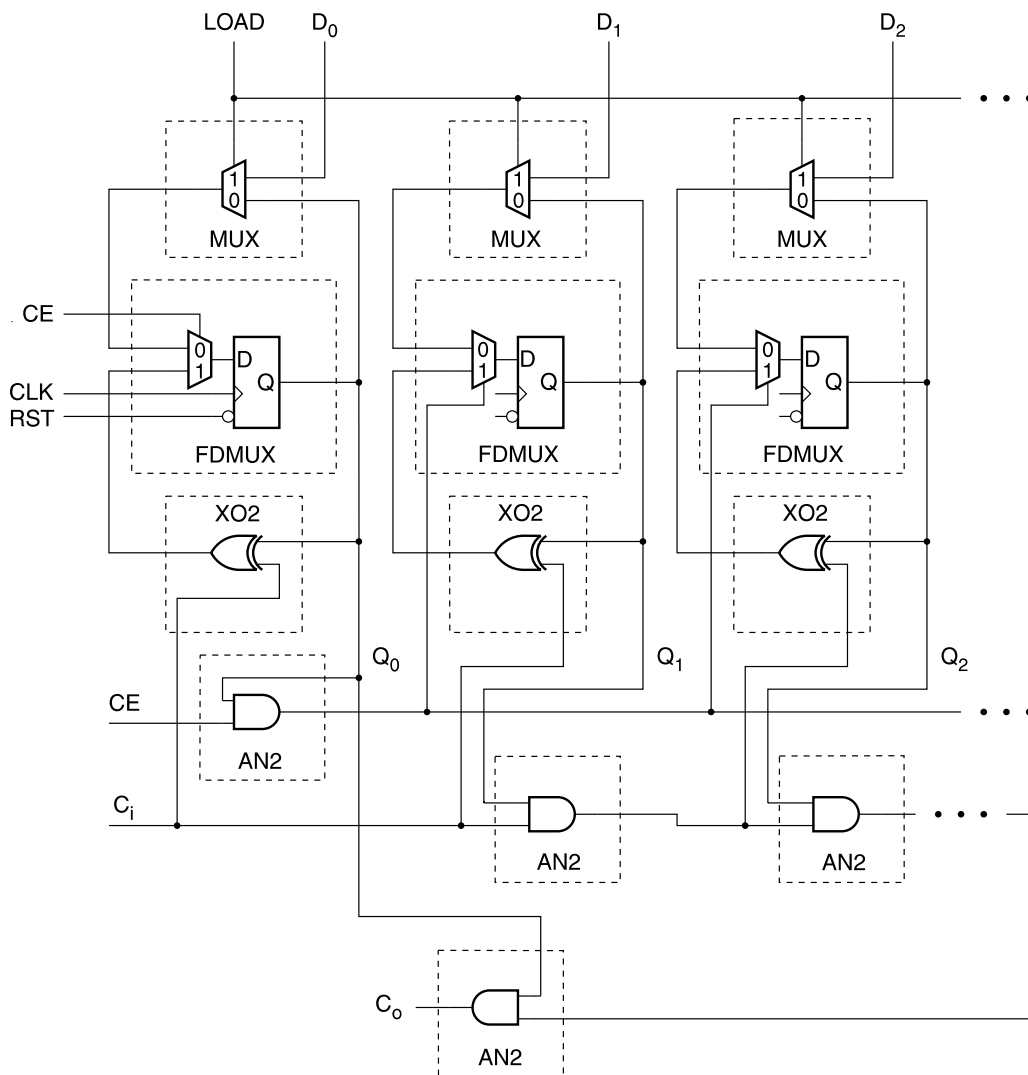


Figure 5. Layout of Counter Architecture

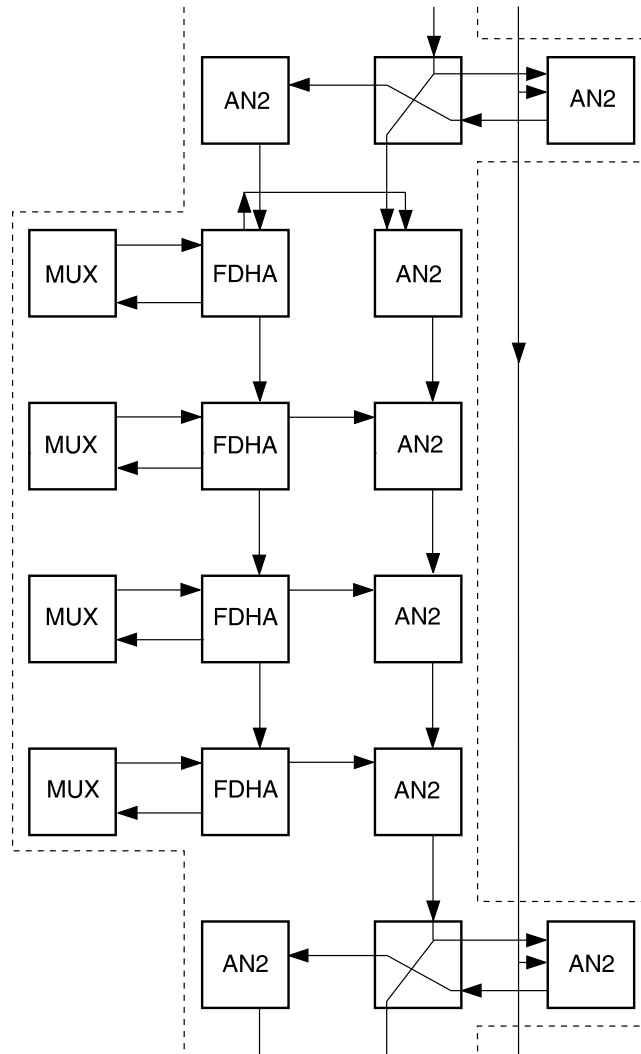


Table 1. Statistics for 16-bit Counter Implementation

Counter	Cell Count ⁽¹⁾	Minimum Bounding Box (X × Y)	Maximum Counting Speed ⁽²⁾	Maximum Loading Speed ⁽³⁾
16-bit	96	17 × 7	14.2 ns/70 MHz	22.7 ns/44 MHz

- Notes:
1. Includes cells used as wires.
 2. Worse-Case Commercial Operating Conditions: CLK → C₀, 70°C, 47.5V.
 3. Worse-Case Commercial Operating Conditions: LOAD → C₀₋₁₅.



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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