AT91SAM7L Microcontroller Series Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM7L series of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM7L Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontroller

Application Note

6369B–ATARM–03-Feb-10

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM7L Series Microcontrollers on Atmel's Web site.

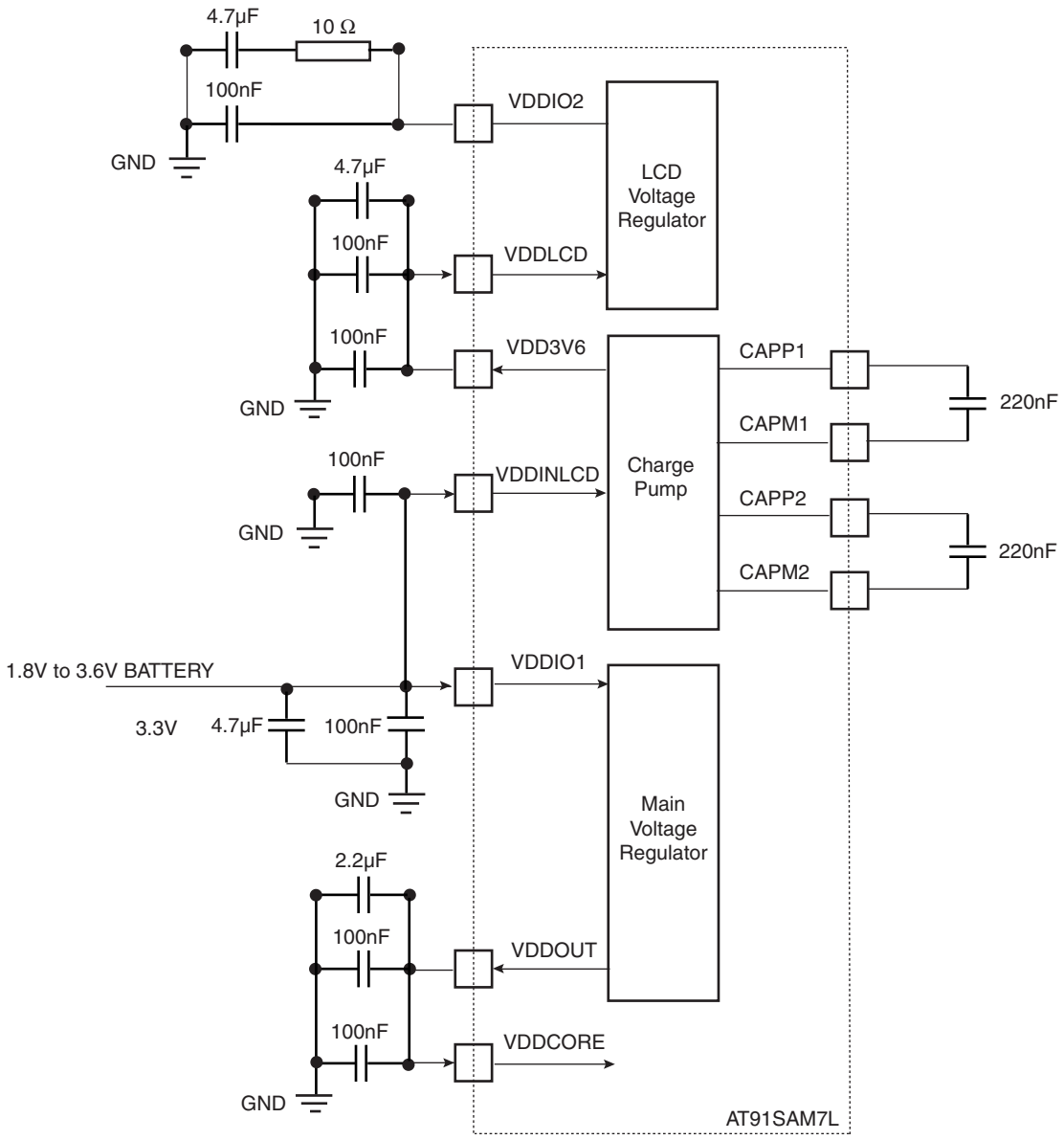
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM7L Series Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI® Datasheet
Evaluation Kit User Guide	AT91SAM7L-EK Evaluation Board User Guide

3. Schematic Check List

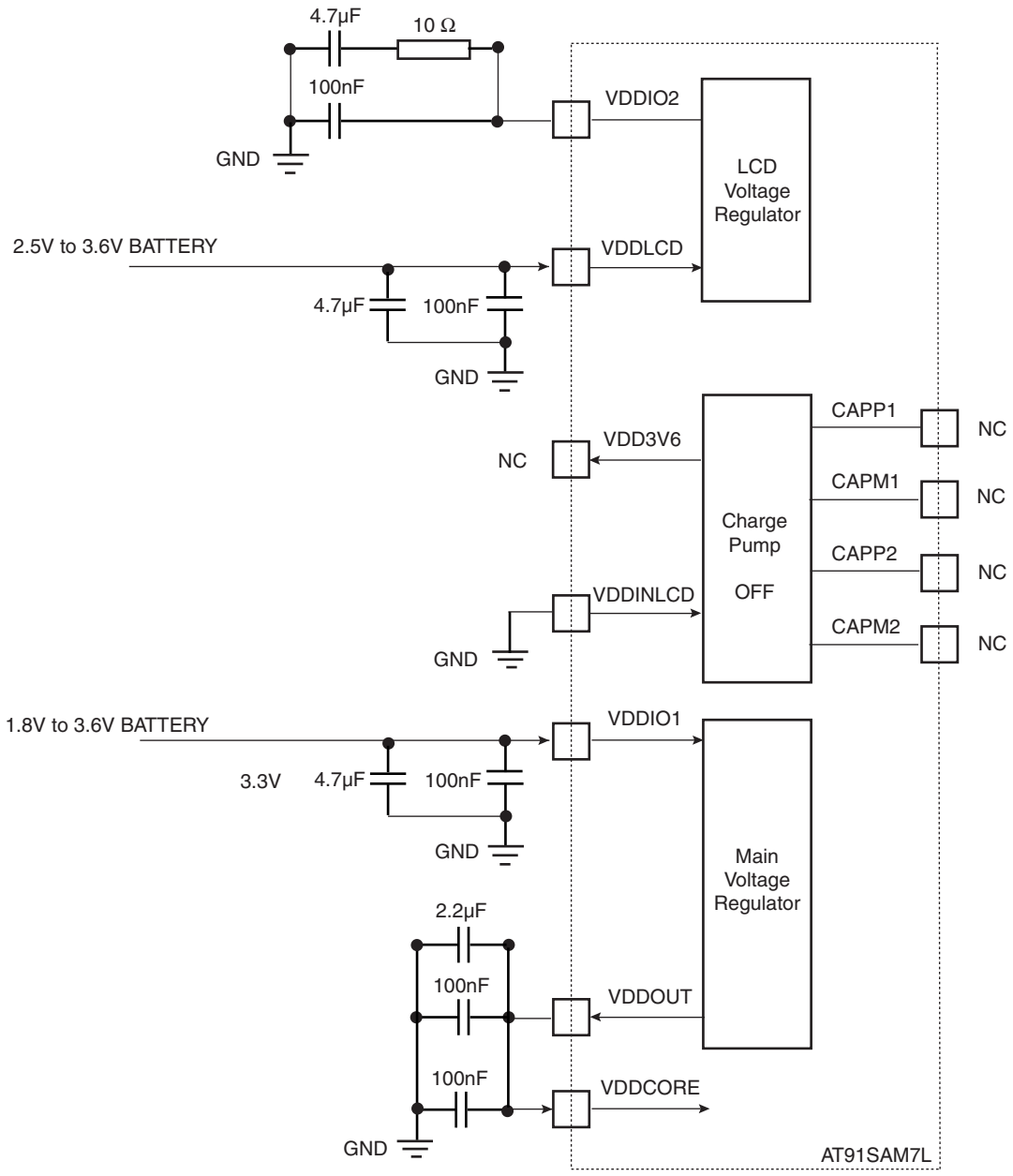
Single Power Supply Strategy



Single Power Supply Schematic Example
Main Voltage Regulator is supplied by battery (1.8V to 3.6V).
Charge Pump supplies the LCD voltage regulator.
LCD voltage regulator is not fed by any power supply.

☑	Signal Name	Recommended Pin Connection	Description
	VDDIO1	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	I/O lines (PIOC) and main voltage regulator power supply Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: Minimum 2.2V at startup**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Output of the main voltage regulator Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling capacitor (100 nF)[1][2]	Core, PLL, Oscillators, ADC and Flash power supply
	VDDIO2	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF) and a 10 Ω resistor[1][2]	LCD I/O lines power supply (PIOA & PIOB) and LCD Voltage regulator output.
	VDDLCD	2.5V to 3.6V Can be connected directly to VDD3V6 pin. Decoupling capacitor (100 nF)[1][2]	LCD Voltage regulator power supply
	VDDINLCD	1.8V to 3.6V Decoupling capacitor (100 nF)[1][2]	Charge pump power supply
	VDD3V6	3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	Charge pump output
	CAPP1	Capacitor needed between CAPP1 and CAPM1 (220 nF)[1]	Charge pump capacitor 1
	CAPM1		
	CAPP2	Capacitor needed between CAPP2 and CAPM2 (220 nF)[1]	Charge pump capacitor 2
	CAPM2		
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as closely as possible to the system ground plane.
	ADVREF	Typically connected to VDDCORE If unused, connected to GND	ADC reference voltage 1.65V to VDDCORE
	AD0-AD3	If unused, connected to GND	Analog inputs 0 to V_{ADVREF}

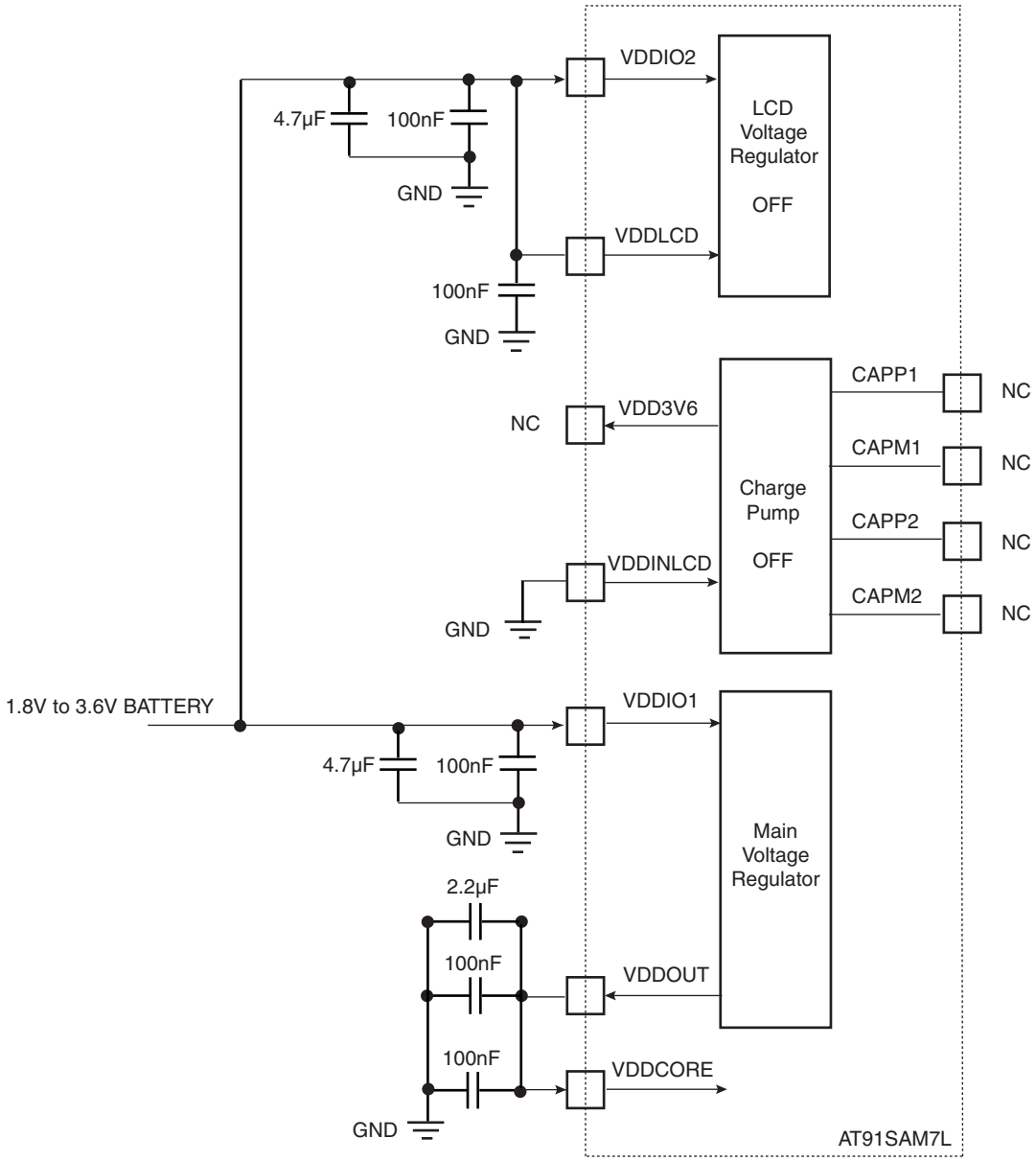
Single Power Supply Strategy: LCD voltage regulator externally supplied.



Dual Power Supply Schematic Example
Main Voltage Regulator is supplied by battery (1.8V to 3.6V).
LCD voltage regulator is externally supplied.
Charge pump is OFF.

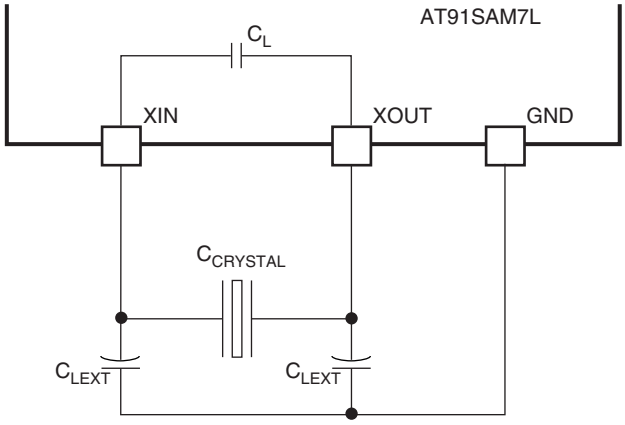
☑	Signal Name	Recommended Pin Connection	Description
	VDDIO1	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	I/O lines (PIOC) and main voltage regulator power supply Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: Minimum 2.2V at startup**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Output of the main voltage regulator Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling capacitor (100 nF)[1][2]	Core, PLL, Oscillators, ADC and Flash power supply
	VDDIO2	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	LCD I/O lines power supply (PIOA & PIOB) and LCD Voltage regulator output.
	VDDLCD	2.5V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	LCD Voltage regulator power supply
	VDDINLCD	Connected to GND	-
	VDD3V6	Can be left unconnected	-
	CAPP1	Can be left unconnected	-
	CAPM1		
	CAPP2	Can be left unconnected	-
	CAPM2		
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as closely as possible to the system ground plane.
	ADVREF	Typically connected to VDDCORE If unused, connected to GND	ADC reference voltage. 1.65V to VDDCORE
	AD0-AD3	If unused, connected to GND	Analog inputs 0 to V_{ADVREF}

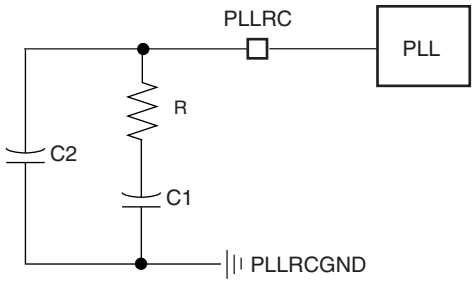
3.3V Single Power Supply Strategy: Charge Pump & LCD Voltage regulator not used



Dual Power Supply Schematic Example
Main Voltage Regulator is supplied by battery (1.8V to 3.6V).
LCD Voltage regulator is unused.
Charge Pump is unused.
Caution: VDDLCD mandatory even if LCD voltage regulator is unused due to design constraint.

☑	Signal Name	Recommended Pin Connection	Description
	VDDIO1	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7 µF)[1][2]	I/O lines (PIOC) and voltage regulator power supply. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. **Warning: Minimum 2.2V at startup**
	VDDOUT	Decoupling/Filtering capacitors (100 nF and 2.2 µF)[1][2]	Output of the main voltage regulator Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling capacitor (100 nF)[1][2]	Core power supply
	VDDIO2	1.8V to 3.6V Decoupling/Filtering capacitors (100 nF and 4.7µF)[1][2]	LCD I/O lines power supply (PIOA & PIOB) and LCD Voltage regulator output.
	VDDLCD	Must be directly connected to VDDIO2 Decoupling capacitors (100 nF)[1][2]	LCD Voltage regulator power supply
	VDDINLCD	Connected to GND	-
	VDD3V6	Can be left unconnected	-
	CAPP1	Can be left unconnected	-
	CAPM1		
	CAPP2	Can be left unconnected	-
	CAPM2		
	GND	Ground	No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as closely as possible to the system ground plane.
	ADVREF	Typically connected to VDDCORE If unused, connected to GND	ADC reference voltage. Must be inferior or equal to VDDCORE
	AD0-AD3	If unused, connected to GND	Analog inputs Must be inferior or equal to VDDCORE

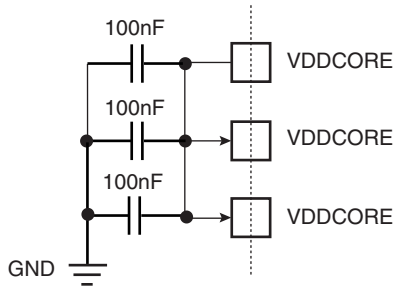
☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT 32 KHz Oscillator in Normal Mode	32 kHz Crystal Capacitors on XIN and XOUT (crystal load capacitance dependant)	Internal Equivalent Load Capacitance (C_L): C_L = 2.5 pF Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to check  Refer to the electrical specifications of the AT91SAM7L series datasheet.
	XIN XOUT 32 KHz Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected.	1.8V to 3.6V square wave signal (VDDIO1) 32 kHz External Clock Source Duty Cycle: 40 to 60%
	XIN XOUT 32 KHz Oscillator when embedded 32 KHz RC oscillator is used	XIN and XOUT can be left unconnected.	When the embedded RC oscillator is enabled, no crystal oscillator is needed.
	CLKIN	If unused, tie to low. Must be tied to V_{VDDIO1} to enter Fast Flash Programming (FFPI) mode.(5)	External main clock 1.8V to 3.6V (voltage reference is VDDIO1) Fmax = 36 MHz

☑	Signal Name	Recommended Pin Connection	Description
	PLLRC	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: “ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  R, C1 and C2 must be placed as close as possible to the pins.
	PLLRCGND	Can be left unconnected if PLL not used. **Warning: do not connect to GND**	PLL ground

☑	Signal Name	Recommended Pin Connection	Description
ICE and JTAG[3]			
	TCK	Pull-up (100 kΩ)[1]	No internal pull-up resistor.
	TMS	Pull-up (100 kΩ[1]	No internal pull-up resistor.
	TDI	Pull-up (100 kΩ)[1]	No internal pull-up resistor.
	TD0	Floating	Output driven at up to V_{VDDIO1}
	JTAGSEL	**In harsh[4] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 KΩ).**	Internal pull-down resistor (15 kΩ). Must be tied to V_{VDDIO1} to enter JTAG Boundary Scan.
Flash Memory			
	ERASE	**In harsh[4] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 KΩ).**	Internal pull-down resistor (15 kΩ). Must be tied to V_{VDDIO1} to erase the General Purpose NVM bits (GPNVMx), the whole flash content and the security bit (SECURITY). This pin is debounced by SCLK to improve the glitch tolerance. Minimum debouncing time is 220 ms. **Warning: VDDCORE is mandatory.**
Reset/Test			
	NRST	Application dependant. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIO1} (100 kΩ) is available for User Reset and External Reset control.
	TST[5]	**In harsh[4] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low-value resistor (such as 1 KΩ).**	Internal pull-down resistor (15 kΩ).
	NRSTB	Can be connected to a push button or to an external reset system **In harsh[4] environments, it is strongly recommended to add an external capacitor (10 nf) between NRSTB and VDDIO1.**	NRSTB is an asynchronous reset input always active. An internal pull-up resistor (10 kΩ) to V_{VDDIO1} is available.
	FWUP	If unused, tie this pin to GND. Add a pull-up resistor (100 kΩ) if OFF Mode or FWUP functionality is used. Must be tied low to enter in Fast Flash Programming (FFPI) mode.[5]	Force wake-up input No internal pull-up resistor.

☑	Signal Name	Recommended Pin Connection	Description
		PIO	
	PAx - PBx	Application Dependant (Pulled-up on V_{VDDIO2})	At 1st power-up, PAx and PBx are in undefined state. At reset, all PIOs are configured as schmitt trigger inputs with pull-up. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
	PCx	Application Dependant (Pulled-up on V_{VDDIO1})	At 1st power-up, PCx is configured as high-impedance input. At reset, all PIOs are configured as schmitt trigger inputs with pull-up. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
5. See: Test Pin description in I/O Lines Considerations section of the AT91SAM7L datasheet for more details on the different conditions to enter FFPI mode.

.

4. AT91SAM Boot Program Hardware Constraints

See AT91SAM Boot Program section of the AT91SAM7L datasheet for more details on the boot program.

4.1 SAM-BA Boot

The SAM-BA® Boot Assistant supports serial communication via the DBGU. No external 32 kHz crystals are needed.

Revision History

Doc. Rev	Comments	Change Request Ref.
6369B	On page 9, C_L = 2.5 pF instead of 6.8 pF.	6929
6369A	First issue	

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

Technical Support
AT91SAM Support
Atmel techincal support

Sales Contacts
www.atmel.com/contacts/

Literature Requests
www.atmel.com/literature