
AT91SAM9R/RL64 Microcontroller Series Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM9R/RL series of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM9R/RL Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.



AT91 ARM Thumb-based Microcontrollers

Application Note

6419C-ATARM-14-Sep-09



2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the [AT91SAM9R/RL](#) Series Microcontrollers on Atmel's Web site.

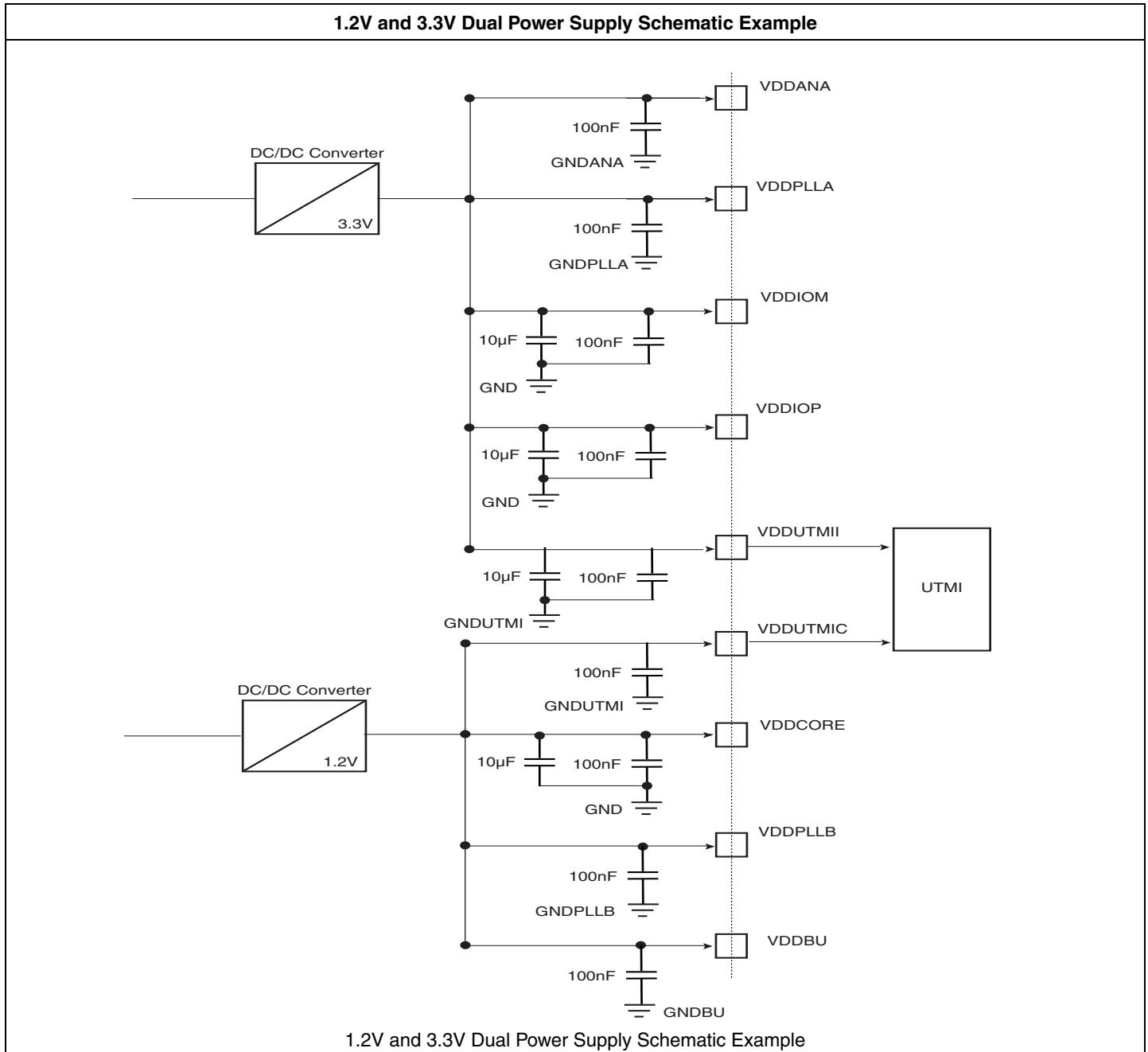
[Table 2-1](#) gives the associated documentation needed to support full understanding of this application note.

Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM9R/RL Series Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	AT91SAM9R/RL-EK Evaluation Board User Guide
Using SDRAM on AT91SAM9 Microcontrollers	Using SDRAM on AT91SAM9 Microcontrollers
NAND Flash Support in AT91SAM9 Microcontrollers	NAND Flash Support in AT91SAM9 Microcontrollers

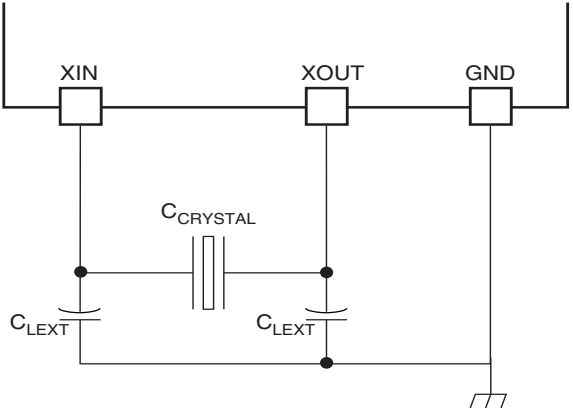
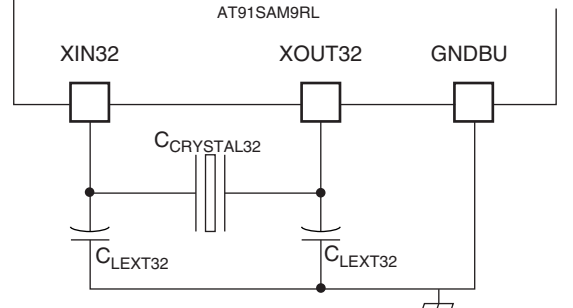
3. Schematic Check List

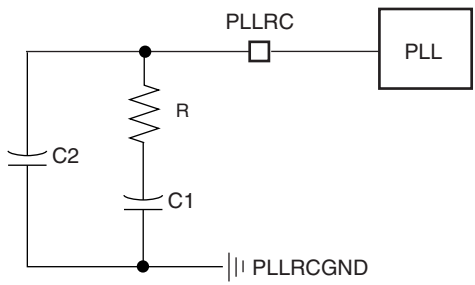
CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the Electrical Characteristics section in the datasheet to guarantee reliable operation of the device.



☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.08V to 1.32V Decoupling/Filtering capacitors (100 nF and 10µF) ⁽¹⁾⁽²⁾	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDBU	1.08V to 1.32V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the Slow Clock oscillator and a part of the System Controller.
	VDDIOM ⁽³⁾	1.65V to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF) ⁽¹⁾⁽²⁾	Powers External Bus Interface I/O lines. Dual voltage range supported. The voltage ranges are selected by programming the VDDIOMSEL bit in the EBI_CSA register. At power-up, the selected voltage is 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP ⁽³⁾	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF) ⁽¹⁾⁽²⁾	Powers Peripheral I/O lines. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLLA	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the PLL cell.
	VDDPLLB	1.08V to 1.32V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the UTMI PLL (480MHz) and OSC 12M cells.
	VDDANA	3.0V to 3.6V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the ADC cell.
	VDDUTMII	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF) ⁽¹⁾⁽²⁾	Powers the UTMI+ interface.
	VDDUTMIC	1.08V to 1.32V Decoupling capacitor (100 nF) ⁽¹⁾⁽²⁾	Powers the UTMI+ core.
	GND	Ground	GND pins are common to VDDCORE, VDDIOM and VDDIOP pins. GND pins should be connected as shortly as possible to the system ground plane.
	GNDPLLA	PLL ground	GNDPLLA pin is provided for VDDPLLA pin. GNDPLLA pin should be connected as shortly as possible to the system ground plane.
	GNDPLLB	UTMI PLL and OSC 12M ground	GNDPLLB pin is provided for VDDPLLB pin. GNDPLLB pin should be connected as shortly as possible to the system ground plane.

<input checked="" type="checkbox"/>	Signal Name	Recommended Pin Connection	Description
	GNDANA	ADC analog ground	GNDANA pin is provided for VDDANA pin. GNDANA pin should be connected as shortly as possible to the system ground plane.
	GNDDBU	Backup ground	GNDDBU pin is provided for VDDDBU pin. GNDDBU pin should be connected as shortly as possible to the system ground plane.
	GNDUTMI	USB UTMI ground	GNDUTMI pin is provided for VDDUTMII and VDDUTMIC pins. GNDUTMI pin should be connected as shortly as possible to the system ground plane.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	<p>XIN XOUT</p> <p>12MHz Main Oscillator in Normal Mode</p>	<p>Crystals between 8 and 16 MHz</p> <p>USB Device peripheral needs a 12 Mhz clock.</p> <p>Capacitors on XIN and XOUT (crystal load capacitance dependent)</p>	<p>Crystal Load Capacitance to check</p> <p>AT91SAM9RL</p>  <p>Example: for an 12 MHz crystal with a load capacitance of $C_{CRYSTAL} = 15 \text{ pF}$, external capacitors are required: $C_{LEXT} = 24 \text{ pF}$.</p> <p>Refer to the electrical specifications of the AT91SAM9R/RL series datasheet.</p>
	<p>XIN XOUT</p> <p>12MHz Main Oscillator in Bypass Mode</p>	<p>XIN: external clock source XOUT: can be left unconnected.</p> <p>USB Device peripheral needs a 12 Mhz clock.</p>	<p>1.2V (VDDPLL) square wave signal</p> <p>External Clock Source up to 50 MHz</p> <p>Duty Cycle: 40 to 60%</p> <p>Refer to the electrical specifications of the AT91SAM9R/RL datasheet.</p>
	<p>XIN32 XOUT32</p> <p>32KHz Oscillator in Normal Mode</p>	<p>32.768 kHz Crystal</p> <p>Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)</p>	<p>Crystal load capacitance to check ($C_{CRYSTAL32}$).</p> <p>AT91SAM9RL</p>  <p>Example: for an 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32} = 12.5 \text{ pF}$, external capacitors are required: $C_{LEXT32} = 17 \text{ pF}$.</p> <p>Refer to the electrical specifications of the AT91SAM9R/RL datasheet.</p>

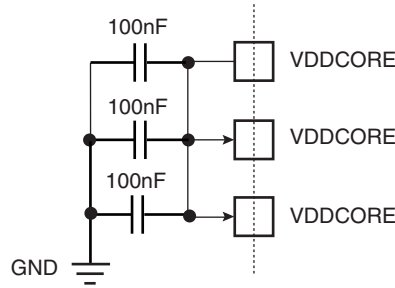
☑	Signal Name	Recommended Pin Connection	Description
	XIN32 XOUT32 32KHz Oscillator in Bypass Mode	XIN32: external clock source XOUT32: can be left unconnected.	1.2V square wave signal (VDDBU) External Clock Source (up to 50MHz) Duty Cycle: 40 to 60%
	PLLRC PLLCA	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: "ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip" (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  <p>R, C1 and C2 must be placed as close as possible to the pins.</p>
ICE and JTAG⁽⁴⁾			
	TCK	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.
	TMS	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.
	TDI	Pull-up (100 kOhm) ⁽¹⁾	No internal pull-up resistor.
	TD0	Floating	Output driven at up to V _{VDDIO1}
	JTAGSEL	In harsh ⁽⁵⁾ environments, it is strongly recommended to tie this pin to GND if not used or to add an external low resistor value (such as 1 kOhm).	Internal pull-down resistor (15 kOhm). Must be tied to V _{DDBU} to enter JTAG Boundary Scan.
	NTRST	Please refer to the I/O line considerations of AT91SAM9R/RL datasheet.	Internal pull-up resistor to V _{VDDIOP} (15 kOhm)
Flash Memory			
	BMS	Application dependent. Must be tied to V _{VDDIOP} to boot on Embedded ROM. Must be tied to GND to boot on external memory (EBI Chip Select 0). Must be stable during boot process.	Internal pull-up resistor to V _{VDDIOP} (100 kOhm).

<input checked="" type="checkbox"/>	Signal Name	Recommended Pin Connection	Description
Reset/Test			
	NRST	Application dependant. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V _{VDDIO1} (100 kOhm) is available for User Reset and External Reset control.
	TST	In harsh ⁽⁵⁾ environments, it is strongly recommended to tie this pin to GND if not used or to add an external low resistor value (such as 1 KOhm).	Internal pull-down resistor (15 kOhm).
	WKUP	0V to VDDBU	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies An external pull-up to VDDBU is needed and its value is to be higher than 1 MOhm. The resistor value is calculated according to the regulator enable implementation and the SHDN level.	The SHDN pin is a tri state output. No internal pull-up resistor. An external pull-up to VDDBU is needed. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).
PIO			
	PAx PBx PCx PDx	Application Dependant	All PIOs are pulled-up inputs at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals: PB10 (A25), PB11 (A18), PB12(A19), PB13 (A20), PB14 (A23), PB15(A24), PB2 (A21), PB3 (A22). Rpullup (typ) = 100 KOhm To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
ADC			
	TSADVREF	2.6V to VDDANA Decoupling/Filtering capacitors. Application dependent.	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used: connect ADVREF to GNDANA.

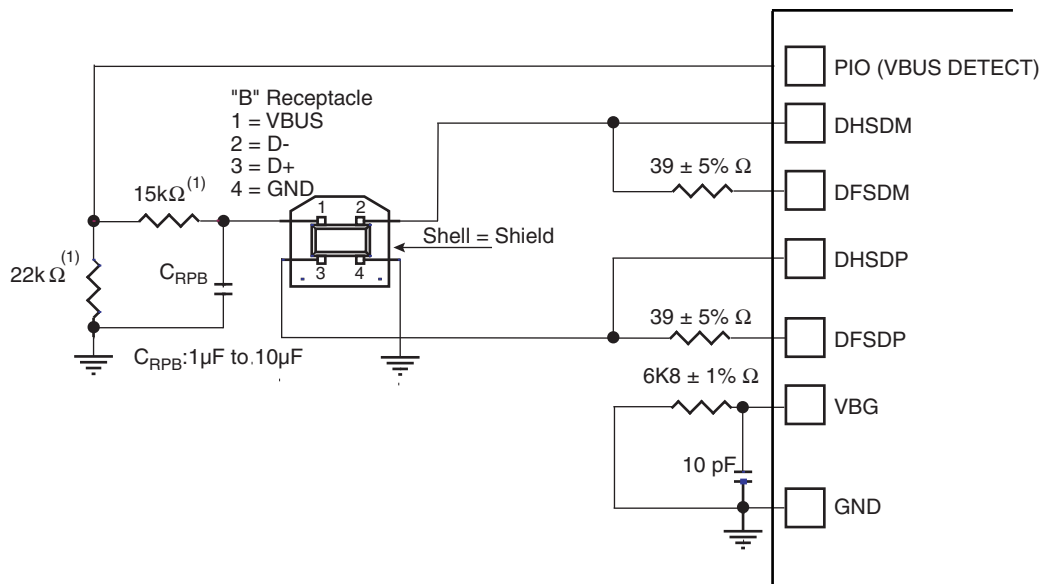
<input checked="" type="checkbox"/>	Signal Name	Recommended Pin Connection	Description
EBI			
	D0-D15 (D16-D31)	Application dependent.	<p>Data Bus (D0 to D31) Data bus lines D0 to D15 are pulled-up inputs to V_{VDDIOM} at reset.</p> <p>Note: Data bus lines D16 to D31 are multiplexed with the PIOC controller. Their I/O line reset state is input with pull-up enabled too.</p>
	A0-A22 (A23-A25)	Application dependent.	<p>Address Bus (A0 to A25) All address lines are driven to '0' at reset.</p> <p>Note: A18 (PB11), A19 (PB12), A20 (PB13), A21 (PB2), A22 (PB3), A23 (PB14), A24 (PB15) and A25 (PB10) are enabled by default at reset through the PIO controllers.</p>
SMC - SDRAM Controller - CompactFlash® Support - NAND Flash Support			
See "External Bus Interface (EBI) Hardware Interface" on page 11.			

<input checked="" type="checkbox"/>	Signal Name	Recommended Pin Connection	Description
USB High Speed Device (UDPHS)			
	DFSDP	Application dependent ⁽⁶⁾	<p>Integrated programmable pull-up resistor. Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected.</p> <p>To reduce power consumption, if USB Device is not used, connect the embedded pull-up.</p>
	DFSDM	Application dependent ⁽⁶⁾	<p>Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected.</p> <p>To reduce power consumption, if USB Device is not used, connect the embedded pull-down.</p>
	DHSDP	Application dependent ⁽⁶⁾	<p>Integrated programmable pull-up resistor. Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected.</p> <p>To reduce power consumption, if USB Device is not used, connect the embedded pull-up.</p>
	DHSDM	Application dependent ⁽⁶⁾	<p>Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected.</p> <p>To reduce power consumption, if USB Device is not used, connect the embedded pull-down.</p>

- Notes:
1. These values are given only as a typical example.
 2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. The double power supplies VDDIOM and VDDIOP power the device differently when interfacing with memories or with peripherals.
4. It is recommended to establish accessibility to a JTAG connector for debug in any case.
5. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
6. Typical USB High Speed Device connection:
As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up. See: Typical-Connection in USB High Speed Device Port section of the [AT91SAM9R/RL datasheet](#) for more details.



4. External Bus Interface (EBI) Hardware Interface

Table 4-1 and Table 4-2 detail the connections to be applied between the EBI pins and the external devices for each Memory Controller:

Table 4-1. EBI Pins and External Static Devices Connections

Signals: EBI_	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	SMC					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB ⁽³⁾	BE0 ⁽⁵⁾
A1/NWR2/NBS2	A1	A0	A0	WE ⁽²⁾	NLB ⁽⁴⁾	BE2 ⁽⁵⁾
A2 - A22	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2	CS	CS	CS	CS	CS	CS
NCS2/NANDCS	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4/CFCS0	CS	CS	CS	CS	CS	CS
NCS5/CFCS1	CS	CS	CS	CS	CS	CS
NRD/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE ⁽¹⁾	WE	WE ⁽²⁾	WE	WE
NWR1/NBS1	–	WE ⁽¹⁾	NUB	WE ⁽²⁾	NUB ⁽³⁾	BE1 ⁽⁵⁾
NWR3/NBS3	–	–	–	WE ⁽²⁾	NUB ⁽⁴⁾	BE3 ⁽⁵⁾

- Notes:
1. NWR1 enables upper byte writes. NWR0 enables lower byte writes.
 2. NWRx enables corresponding byte x writes. (x = 0,1,2 or 3)
 3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
 4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
 5. BEx: Byte x Enable (x = 0,1,2 or 3).

Table 4-2. EBI Pins and External Devices Connections

Signals: EBI0_, EBI1_	Pins of the Interfaced Device			
	SDRAM	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NAND Flash
Controller	SDRAMC	SMC		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0-I/O7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8-I/O15
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21/NANDALE	–	–	–	ALE
A22/NANDCLE	–	REG	REG	CLE
A23 - A24	–	–	–	–
A25	–	CFRNW ⁽¹⁾	CFRNW ⁽¹⁾	–
NCS0	–	–	–	–
NCS1/SDCS	CS	–	–	–
NCS2	–	–	–	–
NCS2/NANDCS	–	–	–	–
NCS3/NANDCS	–	–	–	CE
NCS4/CFCS0	–	CFCS0 ⁽¹⁾	CFCS0 ⁽¹⁾	–
NCS5/CFCS1	–	CFCS1 ⁽¹⁾	CFCS1 ⁽¹⁾	–
NANDOE	–	–	–	OE
NANDWE	–	–	–	WE
NRD/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFCE1	–	CE1	CS0	–
CFCE2	–	CE2	CS1	–

Table 4-2. EBI Pins and External Devices Connections (Continued)

Signals: EBI0_, EBI1_	Pins of the Interfaced Device			
	SDRAM	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NAND Flash
Controller	SDRAMC	SMC		
SDCK	CLK	–	–	–
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx ⁽²⁾	–	CD1 or CD2	CD1 or CD2	–
Pxx ⁽²⁾	–	–	–	CE
Pxx ⁽²⁾	–	–	–	RDY

- Notes:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot..
 2. Any PIO Line.

5. AT91SAM Boot Program Hardware Constraints

See AT91SAM Boot Program section of the [AT91SAM9R/RL datasheet](#) for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals (MHz)

A 12 MHz Crystal is mandatory in order to generate USB and PLL clocks correctly.

5.2 SAM-BA[®] Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-1. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PA21
DBGU	DTXD	PA22

5.3 DataFlash[®] Boot

The DataFlash Boot program searches for a valid application in the SPI DataFlash memory.

The DataFlash must be connected to NPCS0 of the SPI0.

Table 5-2. Pins Driven during DataFlash Boot Program Execution

Peripheral	Pin	PIO Line
SPI0	MOSI	PA26
SPI0	MISO	PA25
SPI0	SPCK	PA27
SPI0	NPCS0	PA28

5.4 SD Card Boot

The SD Card Boot program searches for a valid application in the SD Card memory.

Table 5-3. Pins Driven during SD Card Boot Program Execution

Peripheral	Pin	PIO Line
MCI	MCCK	PA2
MCI	MCCDA	PA1
MCI	MCDA0	PA0
MCI	MCDA1	PA3
MCI	MCDA2	PA4
MCI	MCDA3	PA5

5.5 NAND Flash Boot

The NAND Flash Boot program searches for a valid application in the NAND Flash memory.

Table 5-4. Pins Driven during NAND Flash Boot Program Execution

Peripheral	Pin	PIO Line
PIOD	PIO (for NAND Chip Select)	PB6
PIOB	PIO (for NAND Output Enable)	PB4
PIOB	PIO (for NAND Write Enable)	PB5
Address Bus	NANDCLE	A22
Address Bus	NANDALE	A21

Revision History

Doc. Rev	Comments	Change Request Ref.
6419C	<p>“Clock, Oscillator and PLL” on page 6, updated crystal XIN modification,</p> <p>“USB High Speed Device (UDPHS)” on page 9, updated.</p> <p>“ADC” on page 8 (ADVREF) added.</p>	6596
6419B	Change voltage to XIN XOUT in bypass mode, in Section 3. "Schematic Check List"	rfo
	Add a Caution paragraph before Section 3. "Schematic Check List"	6124
	Change VDDPLL voltage in Section 3. "Schematic Check List"	5905
	Change VDDIOP into VDDBU in JTAGSEL pin description, Section 3. "Schematic Check List"	5862
	Add SHDN (after WKUP) in Section 3. "Schematic Check List"	6419
6419A	First issue	



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