

Migrating to an AT91SAM9G10-based System from an AT91SAM9261S-based System

1. Scope

This application note specifies the migration path from the [AT91SAM9261S](#) to the [AT91SAM9G10](#) microcontroller and describes the differences between them. These variances lie in the Features, Clock Characteristics and Errata.

Note: throughout this document, shaded table cells refer to the AT91SAM9G10.

2. Features

The following list shows the AT91SAM9G10 features that differ from those of the AT91SAM9261S:

- **ARM926EJ-S™ ARM® Thumb® Processor with:**
 - CPU Frequency 266 MHz
- **PIO Controllers**
 - All the I/O Lines are Schmitt Trigger Inputs.
 - all PIO Lines Multiplexed with EBI are VDDIOM Powered
- **Two-wire Interface (TWI)**
 - Compatible with Standard Two-wire Serial Memories
 - One, Two or Three Bytes for Slave Address
 - Sequential Read/Write Operations
 - Master, Multi-master and Slave Mode Operation
 - Bit Rate: Up to 400 Kbits
 - General Call Supported in Slave Mode
 - Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only
- **Multimedia Card Interface (MCI)**
 - SDCard/SDIO and MultiMediaCard™ Compliant
- **LCD Controller Supports**
 - RGB Frame Buffer

All other features apply to AT91SAM9G10 and AT91SAM9261S microcontrollers.

3. Package

The AT91SAM9G10 is available in a 217-ball LFBGA package 15 x 15 mm (0.8 mm ball pitch). The SAM9G10 and the SAM9261S are pin-to-pin compatible.



AT91 ARM Thumb-based Microcontrollers

Application Note



4. PIO Lines Power Supply

4.1 PIOA and PIOC

All IO lines multiplexed with EBI are powered by VDDIOM on an AT91SAM9G10, which allows users to use 1.8V NAND Flash and 1.8V CompactFlash. Other IO lines are not changed.

Table 4-1. PIO Power Supplies

PIO Line	AT91SAM9291S Power Supply	AT91SAM9G10 Power Supply
PA30-PA31	VDDIOP	VDDIOM
PC0-PC7	VDDIOP	VDDIOM

5. Clock Characteristics

5.1 PLL

Table 5-1. PLL Characteristics

PLL Characteristics	AT91SAM9261S	AT91SAM9G10
Range	80 - 240 MHz	80 - 300 MHz
MUL	1 - 1047	1 - 1047
DIV	1 - 255	1 - 255
OUT	00 for 80 - 200 MHz range 10 for 190 - 240 MHz range	00 for 80 - 300 MHz range
Entry Frequency	1 - 32 MHz	1 - 32 MHz
Embedded PLL Filter	No	No

5.2 Processor/Master Clock

Test conditions are defined as follows.

Table 5-2. Test Conditions Definition

Temperature	VDDCORE: 1.2V	VDDIO: 1.8V	VDDIO: 3.3V
85°C	1.08	1.65	3

Table 5-3. Processor/Master Clock

Characteristics	AT91SAM9261S	AT91SAM9G10
Processor Max Frequency	188 MHz	266 MHz
Bus Max Frequency	94 MHz	133 MHz
Master clock divider MDIV	1, 2, 4	1, 2, 4
Current Consumption on VDDCORE in Active Mode	53 mA at 188 / 94 MHz	75 mA at 266 / 133 MHz

5.3 SDRAM Clock

Table 5-4. SDRAM Clocks

Characteristics	AT91SAM9261S	AT91SAM9G10
SDCK Max Frequency at 1.8V (load = 30pF)	94 MHz	133 MHz
SDCK Max Frequency at 3.3V (load = 50pF)		

6. I/O Considerations

It is strongly recommended to place serial resistors (27 or 33 ohms) close to the CPU on all SDRAM signals to prevent:

- Reflection problems and spectral spreading
- Trace ringing

IBIS model can be used to determine the correct value for the resistors according to the PCB.

Refer to the Signal Integrity Application Notes: http://www.atmel.com/dyn/resources/prod_documents/doc6386.pdf, and http://www.atmel.com/dyn/resources/prod_documents/doc6349.pdf

7. LCD Controller

AT91SAM9G10 LCDC is RGB565 compliant whereas AT91SAM9261S LCDC was IBGR555 compliant. AT91SAM9261S users may adapt palette and software or hardware depending on the swapping method they have chosen.

7.1 Palette

The palette is to be updated.

Table 7-1. AT91SAM9261S Lookup Table Structure in the Memory

Address	Data Output [15:0]			
00	Intensity_bit_0	Blue_value_0[4:0]	Green_value_0[4:0]	Red_value_0[4:0]
01	Intensity_bit_1	Blue_value_1[4:0]	Green_value_1[4:0]	Red_value_1[4:0]

Table 7-1. AT91SAM9261S Lookup Table Structure in the Memory (Continued)

Address	Data Output [15:0]			
...				
FE	Intensity_bit_254	Blue_value_254[4:0]	Green_value_254[4:0]	Red_value_254[4:0]
FF	Intensity_bit_255	Blue_value_255[4:0]	Green_value_255[4:0]	Red_value_255[4:0]

Table 7-2. AT91SAM9G10 Lookup Table Structure in the Memory

Address	Data Output [15:0]		
00	Red_value_0[4:0]	Green_value_0[5:0]	Blue_value_0[4:0]
01	Red_value_1[4:0]	Green_value_1[5:0]	Blue_value_1[4:0]
...			
FE	Red_value_254[4:0]	Green_value_254[5:0]	Blue_value_254[4:0]
FF	Red_value_255[4:0]	Green_value_255[5:0]	Blue_value_255[4:0]

7.2 Software Swap

As the swap of blue and red components by software is CPU consuming, about 7.7% of the CPU time is saved by removing this routine. Refer to http://www.atmel.com/dyn/resources/prod_documents/doc6300.pdf

7.3 Hardware Swap

SAM9261S LCDC is based on IBGR555 (Intensity-Blue-Green-Red) standard, where:

- I is the Intensity Bit, and
- B[4:0], G[4:0] and R[4:0] are respectively blue, green and red video components.

The memory map of a pixel in 16-bit mode in the frame buffer is:

I	B4	B3	B2	B1	B0	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0
---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

SAM9G10 LCDC is based on RGB565 (Red-Green-Blue) standard.

The memory map of a pixel in 16-bit mode in the frame buffer is:

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

The LCD lines are to be connected as follows:

Table 7-3. LCD Signal Multiplexing

LCD Data Bus	AT91SAM9261S 24-bit TFT	AT91SAM9261S 18-bit TFT	AT91SAM9261S 16-bit TFT	AT91SAM9G10 24-bit TFT	AT91SAM9G10 18-bit TFT	AT91SAM9G10 16-bit TFT
LCDD[23]	LCD_RED7	LCD_RED5	LCD_RED4	LCD_BLUE7	LCD_BLUE5	LCD_BLUE4
LCDD[22]	LCD_RED6	LCD_RED4	LCD_RED3	LCD_BLUE6	LCD_BLUE4	LCD_BLUE3
LCDD[21]	LCD_RED5	LCD_RED3	LCD_RED2	LCD_BLUE5	LCD_BLUE3	LCD_BLUE2
LCDD[20]	LCD_RED4	LCD_RED2	LCD_RED1	LCD_BLUE4	LCD_BLUE2	LCD_BLUE1
LCDD[19]	LCD_RED3	LCD_RED1	LCD_RED0	LCD_BLUE3	LCD_BLUE1	LCD_BLUE0
LCDD[18]	LCD_RED2	LCD_RED0		LCD_BLUE2	LCD_BLUE0	
LCDD[17]	LCD_RED1			LCD_BLUE1		
LCDD[16]	LCD_RED0			LCD_BLUE0		
LCDD[15]	LCD_GREEN7	LCD_GREEN5	LCD_GREEN4	LCD_GREEN7	LCD_GREEN5	LCD_GREEN5
LCDD[14]	LCD_GREEN6	LCD_GREEN4	LCD_GREEN3	LCD_GREEN6	LCD_GREEN4	LCD_GREEN4
LCDD[13]	LCD_GREEN5	LCD_GREEN3	LCD_GREEN2	LCD_GREEN5	LCD_GREEN3	LCD_GREEN3
LCDD[12]	LCD_GREEN4	LCD_GREEN2	LCD_GREEN1	LCD_GREEN4	LCD_GREEN2	LCD_GREEN2
LCDD[11]	LCD_GREEN3	LCD_GREEN1	LCD_GREEN0	LCD_GREEN3	LCD_GREEN1	LCD_GREEN1
LCDD[10]	LCD_GREEN2	LCD_GREEN0	Intensity Bit	LCD_GREEN2	LCD_GREEN0	LCD_GREEN0
LCDD[9]	LCD_GREEN1			LCD_GREEN1		
LCDD[8]	LCD_GREEN0			LCD_GREEN0		
LCDD[7]	LCD_BLUE7	LCD_BLUE5	LCD_BLUE4	LCD_RED7	LCD_RED5	LCD_RED4
LCDD[6]	LCD_BLUE6	LCD_BLUE4	LCD_BLUE3	LCD_RED6	LCD_RED4	LCD_RED3
LCDD[5]	LCD_BLUE5	LCD_BLUE3	LCD_BLUE2	LCD_RED5	LCD_RED3	LCD_RED2
LCDD[4]	LCD_BLUE4	LCD_BLUE2	LCD_BLUE1	LCD_RED4	LCD_RED2	LCD_RED1
LCDD[3]	LCD_BLUE3	LCD_BLUE1	LCD_BLUE0	LCD_RED3	LCD_RED1	LCD_RED0
LCDD[2]	LCD_BLUE2	LCD_BLUE0		LCD_RED2	LCD_RED0	
LCDD[1]	LCD_BLUE1			LCD_RED1		
LCDD[0]	LCD_BLUE0			LCD_RED0		

8. Errata

The following table gives the AT91SAM9261S errata list, and the status of each erratum in the AT91SAM9G10 (either 'Fixed' or 'Not Fixed').

Table 8-1. Errata List

Errata Section	Errata Description	Status in AT91SAM9G10
Battery Backup	All errata	Not Fixed
Boot ROM	All errata	Not Fixed
Bus Matrix	All errata	Not Fixed
LCD	All errata except 'Screen Shifting After a Reset'	Fixed
	Screen Shifting After a Reset	Not Fixed
MCI	All errata	Fixed
NTRST	All errata	Not Fixed
SDRAM Controller	All errata	Fixed
Serial Peripheral Interface (SPI)	All errata except 'Baudrate set to 1'	Fixed
	Baudrate set to 1	Not Fixed
Serial Synchronous Controller (SSC)	All errata	Not Fixed
Shutdown (SHDC)	All errata	Fixed
System Controller	Possible event loss when reading RTT_SR	Not Fixed
Two-wire Interface (TWI)	All errata	Fixed
Universal Synchronous Asynchronous Receiver Transmitter (USART)	All errata except 'DCD is Active High Instead of Low'	Fixed
	DCD is Active High Instead of Low	Not Fixed
USB Host Port (UHP)	All errata	Not Fixed
USB Device Port (UDP)	All errata	Not Fixed

For a detailed errata description, please refer to the errata section in the [AT91SAM9261S](#) datasheet.

Revision History

Doc. Rev	Comments	Change Request Ref.
6440B	Table 4-1, "PIO Power Supplies," edited	7265
6440A	First issue	



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