AVR188: Design Guidelines for ATtiny43U

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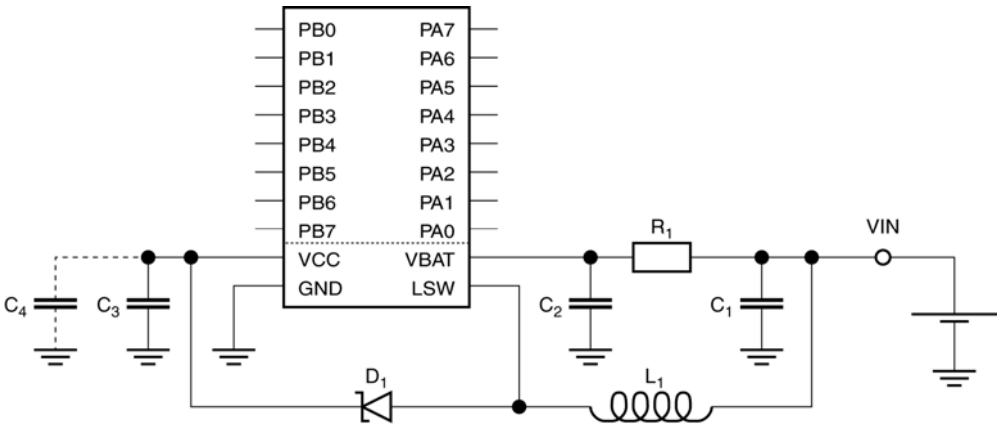
1 Introduction

The integrated boost converter of ATtiny43U provides the microcontroller and peripherals with a fixed supply voltage, generated from an external supply of lower voltage. The boost converter is a switching type, step-up regulator that requires some external components to be complete. This includes an external inductor, a diode and some bypass capacitors. The inductor is connected between the V_{BAT} node and the LSW pin, and the Schottky diode between pins LSW and V_{CC}. In addition, an input capacitor and external bypass capacitor from V_{CC} to GND are usually required.

Figure 1-1. Typical Connection of Boost Converter.



The boost converter continuously switches between storing energy in and draining energy from the external inductor. During the charge phase the current in the inductor ramps up at a rate determined by the converter input voltage. During the discharge phase energy stored in the inductor is released to the load and the current in the inductor ramps down at a rate determined by the difference between the input and output voltages.

8-bit AVR® Microcontrollers

Application Note

Rev. 8206C-AVR-06/10

2 Component Optimization

Table 2-1 below presents component values for a design that has been optimized for high performance. For other component recommendations, see “Typical Component Values” on page 16.

Table 2-1. Recommended Component Values.

Comp.	Value	Note	Package	Part Number
C_1	4.7 µF	ESR < 100 mΩ	0805	GRM219R60J475KE19
C_2 , C_4	100 nF		0603	
C_3	22 µF	ESR < 100 mΩ	0805	GRM21BR60J226ME39
D_1	V_F = 0.35 V	I_R = 7 µA @ 25°C	SOD323	PMEG2005EJ
L_1	15 µH	DCR = 260 mΩ	4 x 4 x 1.8 mm	LPS4018-153MLC
R_1	1 kΩ		0603	

2.1 The Inductor

The LPS series of inductor coils, from Coilcraft, have low DC resistance (DCR) and low core loss. They are shielded and available in relatively small packages. A large number of package options are also available.

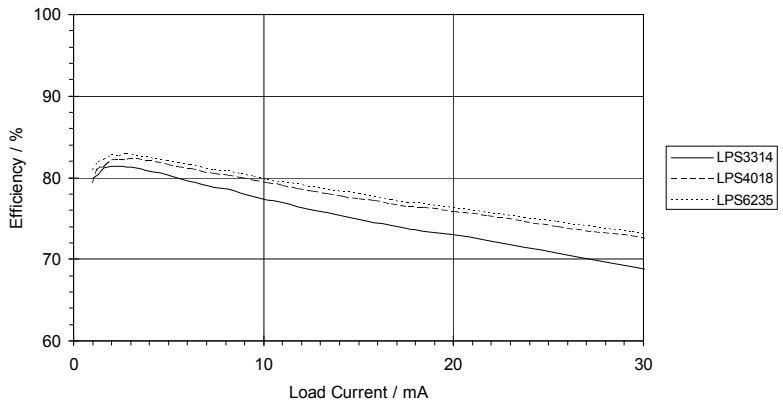
DCR depends on the type and make of inductor. As an example, the DCR of some inductor coils are summarized in Table 2-2 below. The lower the DCR the better the efficiency of the boost regulator.

Table 2-2. Maximum DCR of Some Inductor Coils (Manufacturer’s Data).

Inductor	DCR	Inductance
LPS3314-153MLC	440 mΩ	15 µH
LPS4018-153MLC	260 mΩ	15 µH
LPS6235-153MLC	125 mΩ	15 µH

Figure 2-1 below illustrates how booster efficiency varies with type of inductor and, consequently, DCR. Component values used are those listed in Table 2-1.

Figure 2-1. Booster Efficiency versus Type of Inductor at V_{BAT} = 1.2V and T = 25°C.



Core losses are device specific and are given by coil manufacturers. The lower the core loss the better the efficiency of the boost regulator.

As a rule of thumb, core loss is of importance at low load currents and DCR is of importance at large load currents.

2.2 The Diode

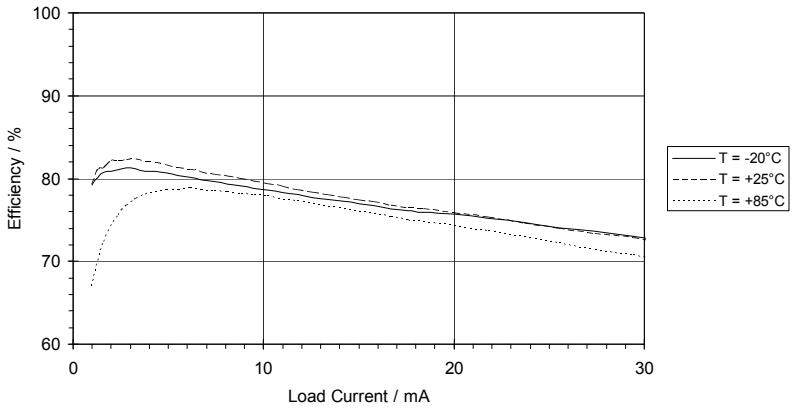
Schottky diodes have low forward voltages (V_F) but relatively high reverse leakage currents (I_R).

Before making a diode selection it is important to know the operating temperature range of the design since forward voltage and reverse leakage current are highly temperature dependent variables. Typically, design dependent trade-offs between V_F and I_R need to be made. For this purpose it is vital to understand how the two parameters affect boost operation, as follows:

- The forward voltage of the diode affects the efficiency at high loads and load currents. The lower the forward voltage the better the efficiency at high currents
- The reverse leakage current affects the Active Low Current Mode of operation and operation at light loads. The lower the reverse leakage current the better the efficiency at low currents

It should be noted that the trade-offs made at room temperature do not necessarily hold at other temperatures. Figure 2-2 below illustrates how booster efficiency depends on temperature. All component values are listed in Table 2-1.

Figure 2-2. Booster Efficiency versus Diode Temperature at V_{BAT} = 1.2V.



The temperature dependency of V_F and I_R are particular to the make and model of diode used. Figure 2-3 below illustrates how booster efficiency at high temperatures is affected by the type of diode used. Component values (excluding the diodes) are those listed in Table 2-1.

Figure 2-3. Booster Efficiency versus Type of Diode. T = 85°C. V_{BAT} = 1.2V.

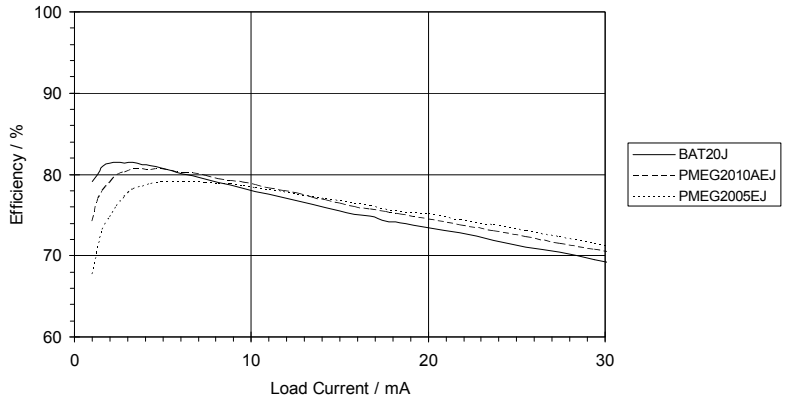


Table 2-3 below shows typical average currents drawn from the battery with two types of diodes and in two operating conditions. In both cases, Power-down Mode with Watchdog Timer disabled and enabled, the boost converter stays in Active Low Current Mode (LCM). Component values (excluding the diodes) are those listed in Table 2-1.

Table 2-3. Typical Average Current Drawn from a Battery in the LCM Mode.

LCM @ T = 25°C, V_{BAT} = 1.2V, FDC = ON	BAT20J (I_R = 0.75 µA)	PMEG2005EJ (I_R = 7.5 µA)
Power-down Mode, Watchdog Timer disabled	2.7 µA	15 µA
Power-down Mode, Watchdog Timer enabled	16 µA	28 µA

Table 2-4 below shows typical average currents drawn from the battery with two types of diodes and five different loading conditions. In all these cases the boost converter stays in Active Regulated Mode.

Table 2-4. Typical Average Current Drawn from a Battery in the Regulated Mode.

Regulated @ T = 25°C, V_{BAT} = 1.2V, FDC = OFF	BAT20J (I_R = 0.75 µA)	PMEG2005EJ (I_R = 7.5 µA)
I_{CC} = 1 mA, Loading Current drawn from V_{CC}	3.2 mA	3.2 mA
I_{CC} = 5 mA	15 mA	15 mA
I_{CC} = 10 mA	32 mA	31 mA
I_{CC} = 20 mA	66 mA	64 mA
I_{CC} = 30 mA	100 mA	97 mA

Total average current ($I_{in,tot}$) drawn from the battery in an application can be calculated with the equation below when the average times (t_x) of the different loading conditions and their input currents ($I_{in,x}$), respectively, are known.

$$I_{in,tot} = \frac{\sum\left(t_x \cdot I_{in,x}\right)}{\sum t_x}$$

3 PCB Layout

Good component placement is important for proper regulator functionality. Following are some guidelines, listed in order of importance:

1. One layer of PCB should be reserved for ground, only. Extended ground areas and vias should have as high conductance as possible.

2. The wires of the LSW node (between LSW pin, inductor L_1 and diode D_1) should be as wide as possible but the area of the node as small as possible. The diode should be close to the inductor.

3. Output capacitor C_3 should be as close to diode D_1 as possible. Similarly, capacitor C_3 (and C_4, if implemented) should be as close to supply (V_{CC}) and ground (GND) pins as possible.

4. Input Capacitor C_1 should be placed as close to inductor L_1 as possible. Also, the tracks from the battery to the input capacitor should be as short as possible. The track going to the battery should have a high conductance because of high current.

5. The capacitor of low-pass-filter (R_1-C_2 in Figure 1-1) should be located as close to the V_{BAT} and GND pins as possible.

PCB tracks should have a high conductance, especially those carrying high current. Table 3-1 below summarizes the high current paths in the design. See Figure 3-1 and Figure 3-2 for recommended track layouts.

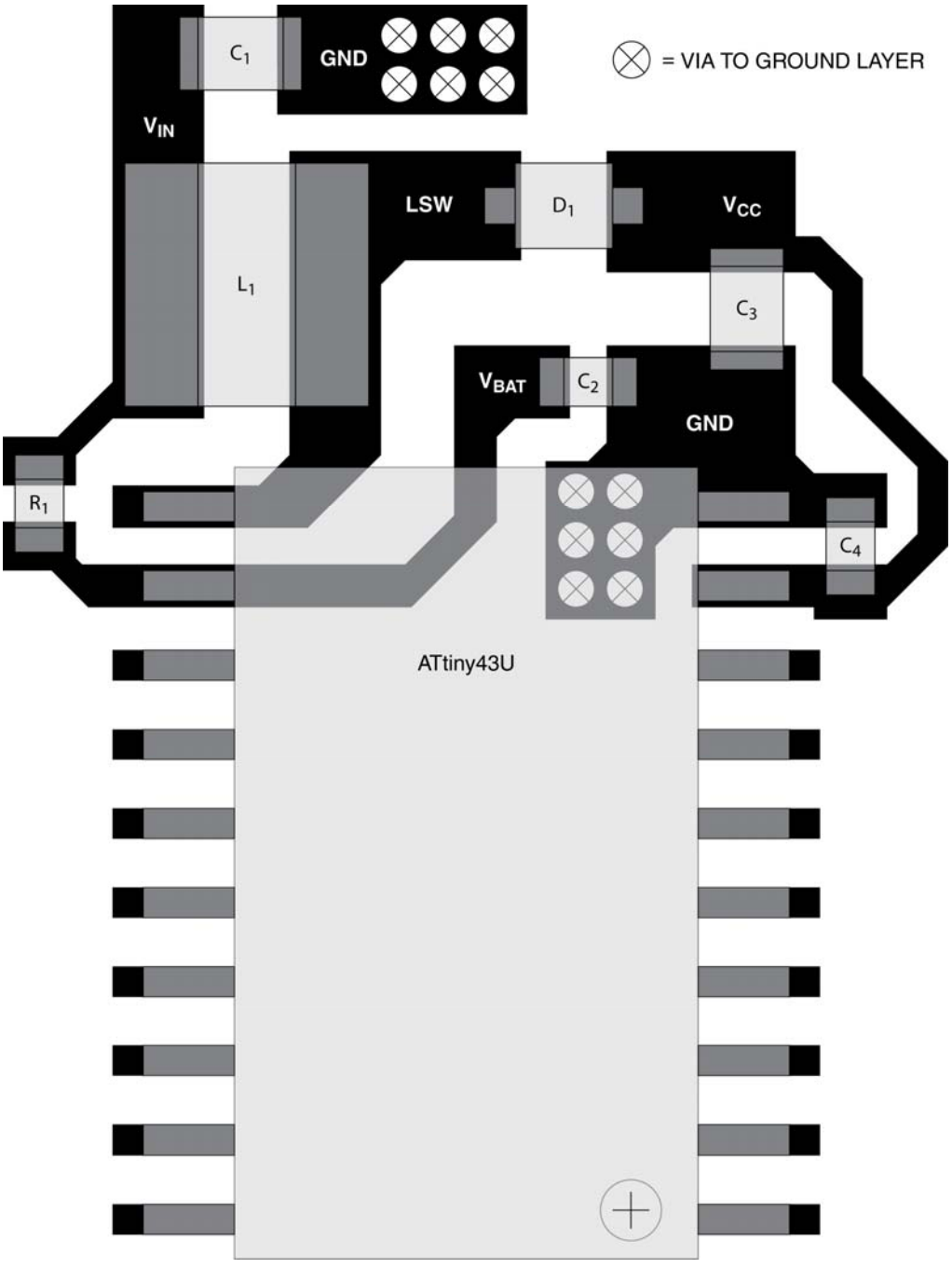
Table 3-1. Paths of High Current.

Current Path	Description	Note
Battery(+) – V_{IN} – L_1 – LSW Pin	Current flow from battery to device during ON time of switching cycle	Current flows here for about 70% of the time
GND Pin – Ground Layer – Battery(-)	Return current to battery during ON time of switching cycle	
Battery(+) – V_{IN} – L_1 – D_1 – C_3	Current flow from battery during OFF time of switching cycle	Current flows here for about 30% of the time
C_3 – Ground Layer – Battery(-)	Return current to battery via ground layer during OFF time of switching cycle	

3.1 SOIC Package

Figure 3-1 below shows an example of the top layer in a design using the ATtiny43U in SOIC package. Component values can be found in Table 2-1.

Figure 3-1. Component Layout Recommendation for SOIC package.

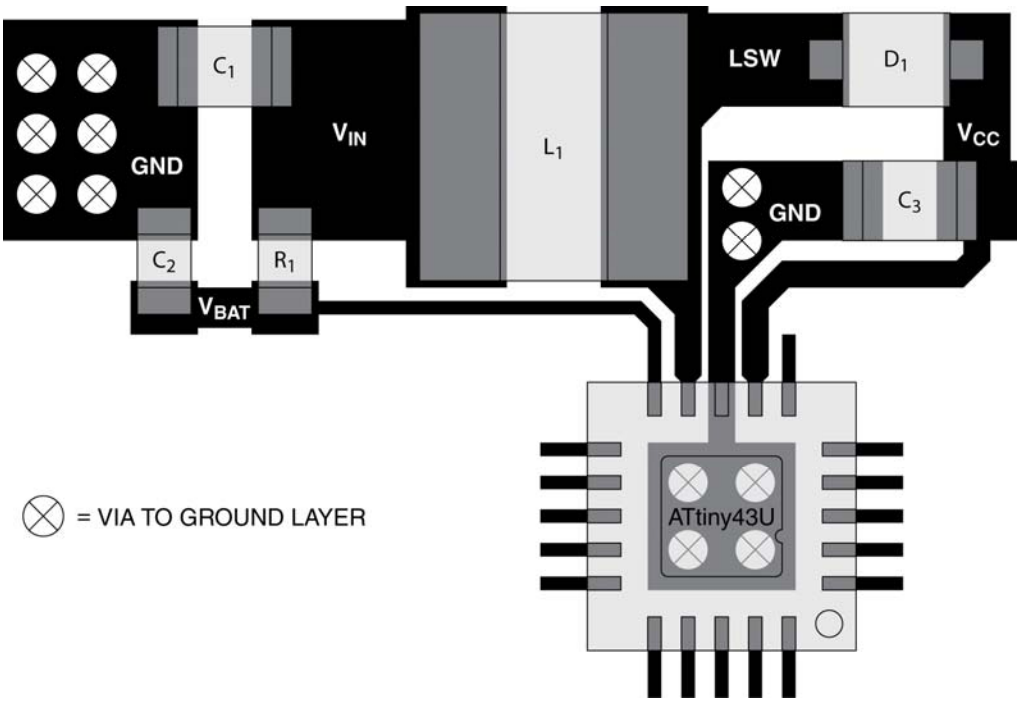


In addition to the top layer, it is also recommended to include a separate ground layer and bolt the ground areas of the top layer to the ground layer firmly by several vias. Ground fillings in the top layer are to be avoided since they are prone to pick up noise.

3.2 MLF Package

Figure 3-2 below shows an example of the top layer in a design using the ATtiny43U in MLF package. Component values can be found in Table 2-1.

Figure 3-2. Component Layout Recommendation for MLF package.

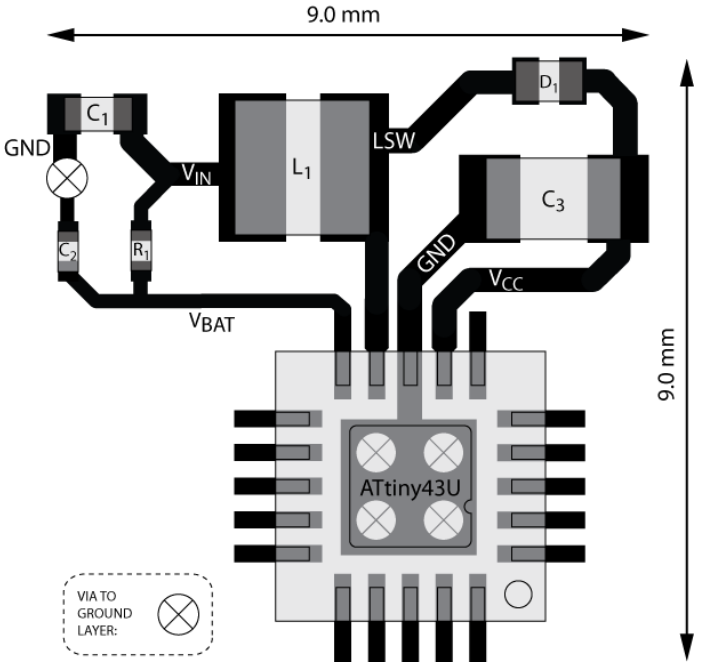


In addition to the top layer, it is also recommended to include a separate ground layer and bolt the ground areas of the top layer to the ground layer firmly by several vias. The exposed die pad of the MLF package should be connected to the ground layer through via matrices. Ground fillings in the top layer are to be avoided since they are prone to pick up noise.

3.3 Minimum Layout

Figure 3-3 below shows a proven example of minimum layout, that can be used with certain trade-offs of specifications. The layout is made for the smallest components available, and narrow wire widths and spacing on PCB.

Figure 3-3. Dedicated Minimum Layout.



The spacing between components in this layout is 1 mm in minimum. Depending on the selected component mounting process the spacing can be adjusted accordingly. The line widths are 0.3 mm in the power path (V_{IN}, LSW, V_{CC} and GND wires). The line thickness should be selected so that the wires can sustain RMS currents of up to 250 mA.

The new EPL and XPL inductor series from Coilcraft utilize very small packages, but they are available only with inductance values of up to 10 µH. However, the ATtiny43U can be used with a 10 µH (±20%) inductor with certain limitations. The lower inductance value causes the current to ramp up faster and higher than with the nominal 15 µH inductor, causing higher losses in the power path. Due to these losses, the temperature of the components and wires increases few degrees (C) with full load.

The components for this minimum layout and its tighter specifications are shown in the Table 3-2 below.

Table 3-2. Components and Specification Limitations for the Minimum Layout.

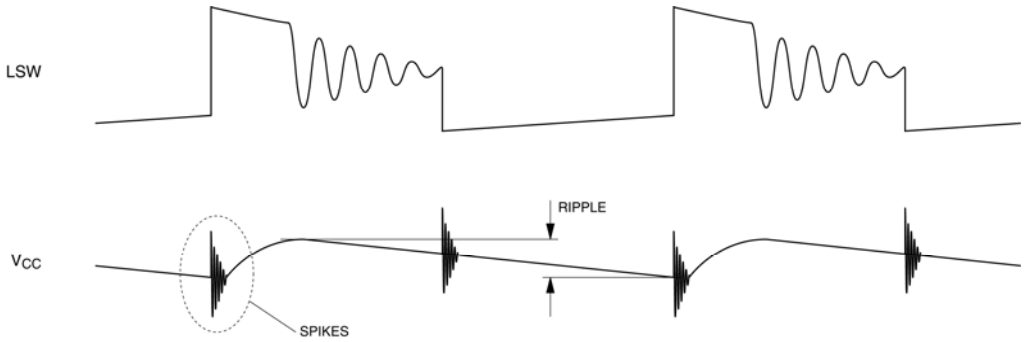
Comp.	Value	Note	Package	Part Number
C_1	4.7 µF		0402	GRM155R60G475ME
C_2	22 nF		0201	GRM033R60J223KE01D
C_3	22 µF		0805	GRM21BR60J226ME39
D_1	V_F = 0.45 V	I_R = 2 µA @ 25°C	SOD882	PMEG2005EL
L_1	10 µH	DCR = 460 mΩ	2 x 2 x 1.4 mm	EPL2014-103MLC
R_1	1 kΩ		0201	RC0201JR-071KL
Maximum Load Current			I_{LOAD} (Max) = 20 mA	
Maximum Input Voltage			V_{BAT} (Max) = 1.6 V	

With this layout the physical size is reduced to minimum, but the specification limits and the efficiency of the converter are somewhat reduced.

4 Smoothing the Supply Voltage

High-frequency voltage spikes appear in supply voltage (V_{CC}) at moments when the inductor is switched on and off, as illustrated in Figure 4-1 below. Low-frequency voltage variation between spikes is referred to as ripple.

Figure 4-1. Typical Voltage Spikes and Ripple at V_{CC} .



Supply voltage ripple and spikes do not affect the operation of the boost regulator but may be undesired in some applications.

The amplitude of V_{CC} ripple mainly depends on the following factors:

- Magnitude of load current. The larger the load current the larger the voltage ripple
- Size and number of output capacitors. Voltage ripples can typically be kept reasonable by using a combination of large and small capacitors
- Quality of output capacitors. Low ESR reduces voltage ripple

The amplitude of V_{CC} spikes depends on the following factors:

- Actual PCB layout. Poor layout and long tracks increases spike magnitudes and may introduce longer periods of ringing. Output capacitors should be placed as close as possible to the V_{CC} pin
- Quality of output capacitors. Low ESL reduces spikes

Table 4-1 below shows typical voltage ripple that can be expected. Please note that actual voltage ripple is highly application dependent and does vary.

Table 4-1. Typical V_{CC} Voltage Ripple.

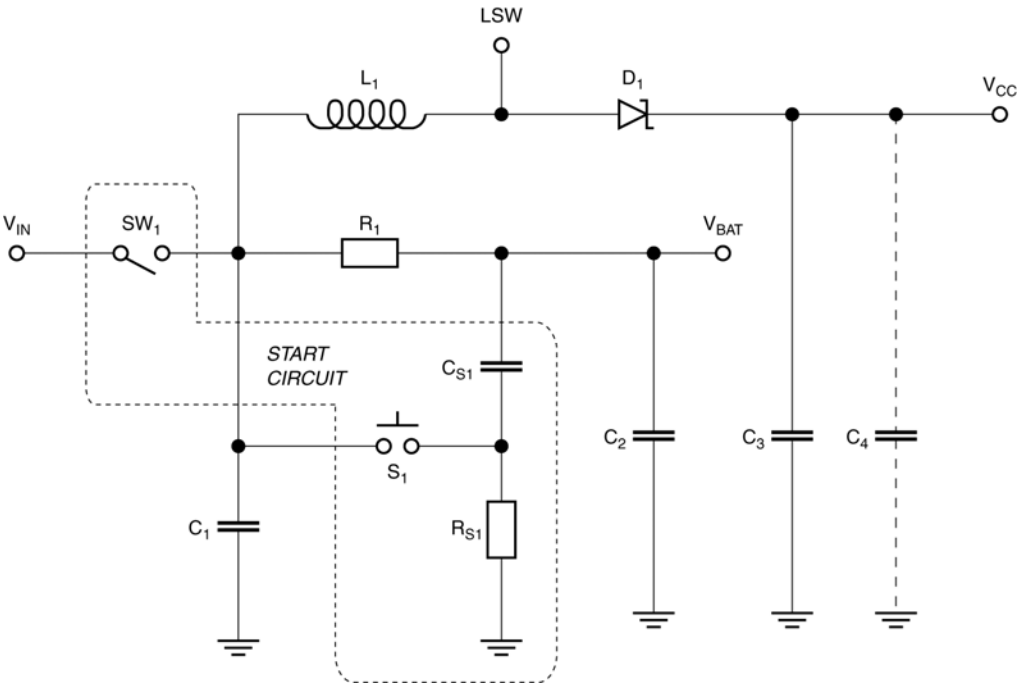
Load Current	V_{CC} Filter Capacitors	Typical V_{P-P} Spikes	Typical V_{P-P} Ripple
1.5 mA	100 nF || 22µF	10 mV	5 mV
30 mA	22 nF || 47µF	20 mV	20 mV
	100 nF || 22µF	30 mV	40 mV
	22 nF || 22µF	40 mV	40 mV
	4.7 nF || 22µF	60 mV	40 mV
	22µF	100 mV	40 mV

5 Start Circuit for Low Voltages

The minimum operating voltage of the boost converter is lower than the start voltage. During normal operation battery charge will drop and, as a result, so will battery voltage. When battery voltage has dropped below boost start voltage a disruption of supply voltage may leave the application in a state where battery voltage is too low for the boost converter to start. Disruptions in supply voltage are unwanted but may occur when, for example, the battery driven application is accidentally dropped.

It is possible to recover and continue operation in situations where battery voltage has already been depleted below boost converter start level. One method for recovery is to implement a low voltage start button, as illustrated in Figure 5-1 below. The actual start circuit is outlined with a dotted line.

Figure 5-1. Schematic of Boost Converter Circuit with Low Voltage Start.



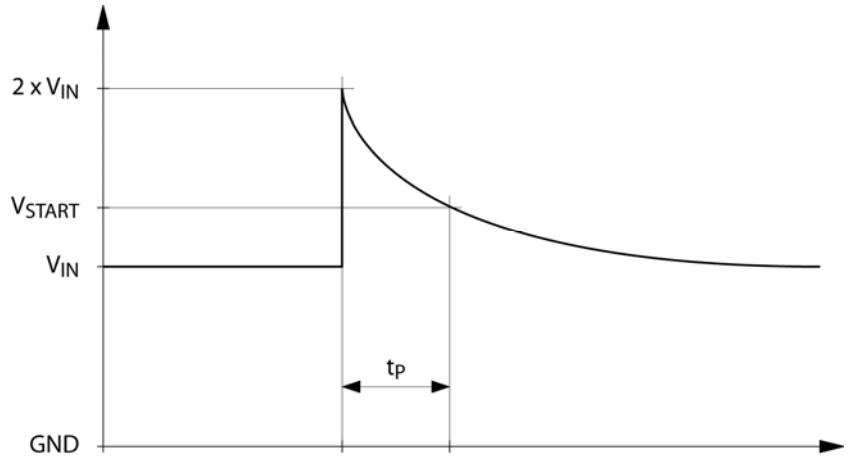
When button, S_1, is pushed the supply voltage is momentarily raised to a level above start voltage, allowing the boost converter to start.

5.1 Operation

When a battery is applied to V_{IN} all capacitors start to charge and voltage at V_{BAT} quickly ramps up to the battery voltage level. After capacitors have charged, and assuming $C_1 = C_{S1}$, pushing button S_1 connects the two capacitors in series, briefly doubling the voltage at V_{BAT} and helping the boost converter to start.

After reaching its maximum the voltage at V_{BAT} starts to drop, as illustrated in Figure 5-2 below.

Figure 5-2. Typical Start Pulse at V_{BAT} , Generated when S_1 Pressed.



For the low voltage start circuitry to be successful the voltage at V_{BAT} needs to remain above the start level V_{START} sufficiently long. The time required, t_P, depends on the battery voltage and the peak amplitude. Typical values are summarized in Table 5-1 below. The values given assume a worst-case start voltage of 1.35V. Actual values may be lower.

Table 5-1. Typical Pulse Widths Required for Low Voltage Start.

Battery Voltage, V_{IN}	Pulse Width, t_P
0.7 V	5 ms
0.8 V	3 ms
0.9 V	1 ms
1.0 V	0.1 ms

Switch SW_1 provides the means for preventing the design from draining the battery during long shell times. In its simplest form this can be a piece of isolating tape between the battery pole and the connector, and simply pulled away when the design is taken into use.

5.2 Component Values

Component values given in Table 5-2 result in a start pulse that is above 1.35V for at least 0.3ms, provided battery voltage is at least 1V. This is sufficient for starting the boost converter.

The start pulse can be prolonged by increasing R_1 but care should be taken to keep the low-pass filter R_1-C_2 within limits. Also, when using the ADC to measure battery voltage the size of R_1 needs to be observed. See device data sheet for more details.

Pulse width can be increased also by increasing the size of C_{S1}.

Table 5-2. Typical Component Values for $V_{IN} \geq 1V$.

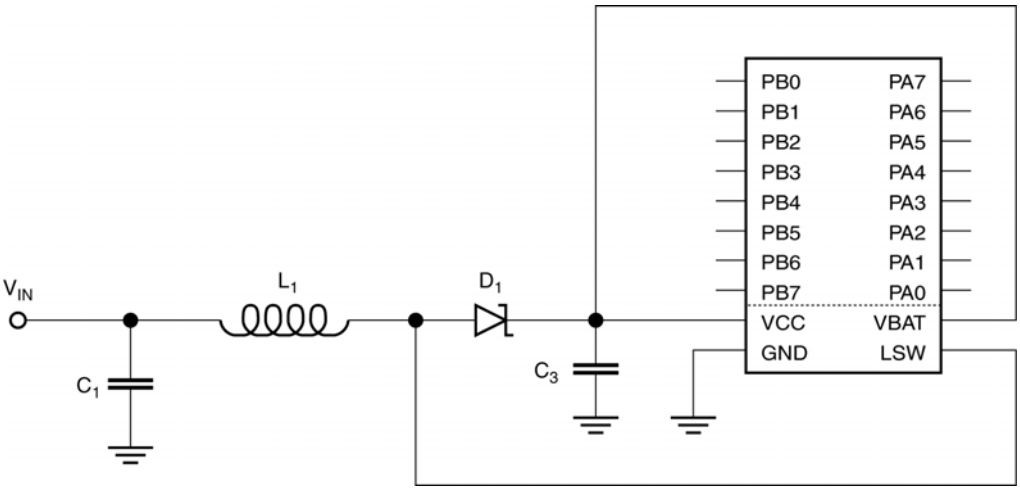
Component	Typical Value
C_1, C_{S1}	2.2 µF
C_2	100 nF
C_3	Not critical
C_4	
D_1	
L_1	
R_1	680 Ω
R_{S1}	100 kΩ

6 Bypassing Hardware Shutdown

It is possible to configure the boost converter such that it does not enter Stop Mode when battery voltage drops below shutdown voltage. This allows the design to drain the battery cell completely. This procedure is recommended for non-rechargeable batteries, only. It should be noted, that draining the battery is harmful for most rechargeable battery chemistries.

Hardware shutdown of boost converter is bypassed by connecting V_{BAT} to a voltage source that does not drop below shutdown voltage. The most obvious choice is to short V_{BAT} to V_{CC}, as shown in Figure 6-1 below. This connection allows enough voltage from V_{IN} to V_{BAT} for the boost converter to start and keeps V_{BAT} as high as possible once the converter is up and running. In this mode of operation the boost regulator can not be stopped by firmware.

Figure 6-1. Schematic for Battery Drain Configuration.



When battery is drained the boost converter input voltage drops and the efficiency of the converter decreases. This means that at lower input voltages more input current is required to generate the same load current. It also means that at lower voltages the maximum load current the boost converter can provide decreases. This is illustrated in Table 6-1 below, where I_{LOAD} is the maximum current the boost converter can provide while still maintaining regulation.

Table 6-1. Typical Supply and Load Currents with Hardware Control Bypassed.

Input Voltage, V_{IN}	Load Current, I_{LOAD} (1)	Input Current, I_{IN} (2)
0.6 V	11 mA	80 mA
0.5 V	8 mA	70 mA
0.4 V	5 mA	60 mA
0.3 V	2.5 mA	45 mA
0.2 V	1 mA	30 mA

Notes: 1. Max current the converter can provide while maintaining regulation (V_{CC} > 2.7V)
2. Current drawn from source at given load current

7 Low Voltage Design with Turn-Off Switch

This design combines the previously described low voltage and battery drain techniques. It also includes a two-pole, two-position switch, which allows the design to be completely turned off, thus extending battery life. The design is illustrated in Figure 7-1, below. Component values are listed in Table 7-1.

Figure 7-1. Schematic for Low Voltage and Battery Drain Configuration.

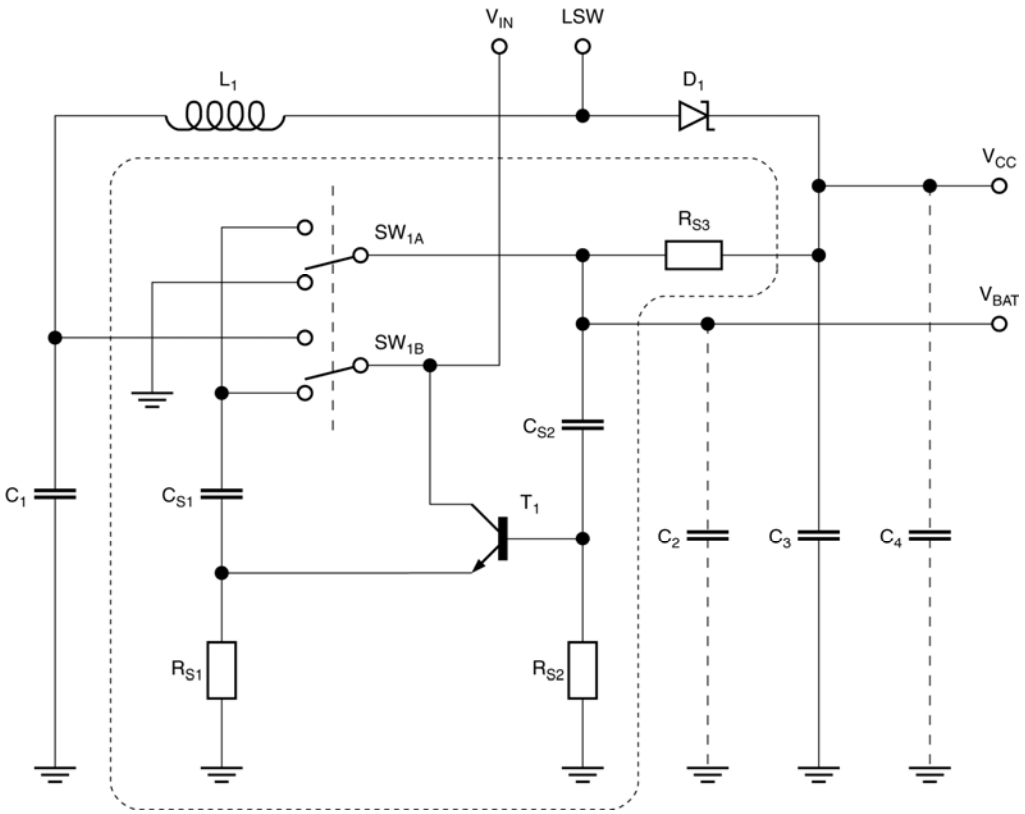


Table 7-1. Component Values.

Component	Value	Note
C_1	4.7 µF	
C_3	22 µF	
C_{S1}	1 µF	
C_{S2}	0.47 µF	
D_1	(not critical)	See page 3 for design guidelines
L_1	(not critical)	See page 2 for design guidelines
R_{S1}	220 kΩ	
R_{S2}	470 kΩ	
R_{S3}	22 kΩ	
T_1	BC847C	NPN

8 Typical Component Values

A typical use of the boost converter is illustrated in Figure 1-1, on page 1. Components can be optimized depending on the type of application, as discussed in section *Component Optimization*, on page 2. The Table 8-1 below presents recommendations for three types of applications (with emphasis on high performance, optimized area and cost effective). All values are guidelines, only. Components with similar specifications from other manufacturers can be used also.

Table 8-1. Typical Component Values vs. Design Emphasis.

Part	Design Emphasis		
	High Performance	**Small Area**	**Low Cost**
C_1	GRM219R60J475KE19 (1)	GRM155R60G475ME (2)	≥ 2 µF
C_2	100 nF	100 nF (2)	– (3)
C_3	GRM21BR60J226ME39 (1)	GRM21BR60J226ME39 (1)	≥ 20 µF
C_4	100 nF	– (4)	– (4)
D_1	PMEG2005EJ (5)	PMEG2005EL (6)	I_{RMS} (Max) ≥ 0.5 A
L_1	LPS4018-153MLC	LPS3314-153MLC	I_{RMS} (Max) ≥ 0.5 A
R_1	1 kΩ	1 kΩ (2)	– (3)

Notes:
1. Package: 0805
2. Package: 0402
3. Increases voltage ripple at VBAT pin.
4. Not required, if MLF packaged device used.
5. Use BAT20J for very low input currents in LCM mode, see Table 2-3 on page 4.
6. Package: SOD882

9 Firmware Example

The assembly code below illustrates how to use the ADC to monitor the battery voltage and shut down the boost regulator when voltage drops below a given threshold. The code example is written for AVR Studio Assembler.

```
;***************************************************************************
; Program: ATtiny43U_ADC_STOP_example
; $Date: 2010/06/01 12:00:00 $
; $Revision: 1.2 $
;***************************************************************************

.include    "tn43Udef.inc"

.def temp    =r16                ; Temporary registers
.def temp2   =r17
.def tempL   =r18                ; Temporary ADC low byte
.def tempH   =r19                ; Temporary ADC high byte
.def accL    =r20                ; Accumulator low byte
.def accH    =r21                ; Accumulator high byte

     rjmp    RESET               ; Reset Handler

.org 0x0080

RESET:
     ldi     temp,   0x5f        ; Set stack pointer
     ldi     temp2,  0x01
     out     SPL,    temp
     out     SPH,    temp2
     rjmp    ADC_VBAT

ADC_VBAT:
     ldi     temp,   0b01000110  ; Int 1.1V Ref and VBAT
     out     ADMUX,  temp
     ldi     temp,   0b10000011  ; Enable ADC and prescaler mclk/8 1MHz
     out     ADCSRA, temp
     ldi     temp,   0b00000000  ; ADLAR bit cleared
     out     ADCSRB, temp

ADC_start:
     ldi     accL,   0x00        ; Clear accumulator accH:accL
     ldi     accH,   0x00
```

```
    rcall   Make_conversion       ; Make 1'st conversion
    add     accL,   tempL
    adc     accH,   tempH

    rcall   Make_conversion       ; Make 2'nd conversion
    add     accL,   tempL
    adc     accH,   tempH

    rcall   Make_conversion       ; Make 3'rd conversion
    add     accL,   tempL
    adc     accH,   tempH

    rcall   Make_conversion       ; Make 4'th conversion
    add     accL,   tempL
    adc     accH,   tempH

    lsr     accH                  ; Divide result by 4
    ror     accL
    lsr     accH
    ror     accL
; 10-bit average result in registers accH:accL

    lsr     accH                  ; Skip 2 LSB bits from 10-bit average
    ror     accL
    lsr     accH
    ror     accL                  ; 8-bit result in register accL

; Use internal 1.1V (typical) reference to check if VBAT is below
; 8-bit stop level
;   0x74 ~ 1.0V
;   0x68 ~ 0.9V
;   0x5d ~ 0.8V
    cpi     accL,   0x68          ; If VBAT < 0.9V,
    brlo    Stop_boost            ; then stop boost

    rjmp    ADC_start

Make_conversion:
    sbi     ADCSRA, ADSC
Wait_conversion_ready:
    sbic    ADCSRA, ADSC
    rjmp    Wait_conversion_ready
    in      tempL,  ADCL
    in      tempH,  ADCH
    ret
```

```
Stop_boost:
     ldi     temp,   0x00           ; Disable all outputs
     out     DDRA,   temp
     out     DDRB,   temp

     ldi     temp,   0b01000000     ; 1.1Vref and ADC0
     out     ADMUX,  temp
     ldi     temp,   0b00000000     ; Disable ADC
     out     ADCSRA, temp

; Boost stop sequence
    ldi     temp,   0b11000000
    out     PRR,    temp
    ldi     temp,   0b10000000
    out     PRR,    temp
    ldi     temp,   0b01000000
    out     PRR,    temp
     rjmp    Read_Boost_Status

Read_Boost_Status:                  ; Poll boost status bit.
     sbis    ADCSRB, 7              ; Jump to reset if boost is restarted
     rjmp    Read_Boost_Status      ; before mcu core POR or BOD reset
     rjmp    RESET
```

10 Table of Contents

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
http://www.atmel.com/

Technical Support
avr@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Request
www.atmel.com/literature