AVR188: Design Guidelines for ATtiny43U

Features

- Overview of Boost Converter Operation
- Optimizing Component Values
- Recommendations for PCB Layout
- Reducing Ripples and Spikes in Supply Voltage
- Building a Start Circuit for Low Voltages
- Bypassing Hardware Control and Draining Batteries Completely
- Firmware Example

1 Introduction

The integrated boost converter of ATtiny43U provides the microcontroller and peripherals with a fixed supply voltage, generated from an external supply of lower voltage. The boost converter is a switching type, step-up regulator that requires some external components to be complete. This includes an external inductor, a diode and some bypass capacitors. The inductor is connected between the \( V_{BAT} \) node and the LSW pin, and the Schottky diode between pins LSW and \( V_{CC} \). In addition, an input capacitor and external bypass capacitor from \( V_{CC} \) to GND are usually required.

Figure 1-1. Typical Connection of Boost Converter.

The boost converter continuously switches between storing energy in and draining energy from the external inductor. During the charge phase the current in the inductor ramps up at a rate determined by the converter input voltage. During the discharge phase energy stored in the inductor is released to the load and the current in the inductor ramps down at a rate determined by the difference between the input and output voltages.
2 Component Optimization

Table 2-1 below presents component values for a design that has been optimized for high performance. For other component recommendations, see "Typical Component Values" on page 16.

Table 2-1. Recommended Component Values.

<table>
<thead>
<tr>
<th>Comp.</th>
<th>Value</th>
<th>Note</th>
<th>Package</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₁</td>
<td>4.7 µF</td>
<td>ESR &lt; 100 mΩ</td>
<td>0805</td>
<td>GRM219R60J475KE19</td>
</tr>
<tr>
<td>C₂, C₄</td>
<td>100 nF</td>
<td></td>
<td>0603</td>
<td></td>
</tr>
<tr>
<td>C₃</td>
<td>22 µF</td>
<td>ESR &lt; 100 mΩ</td>
<td>0805</td>
<td>GRM21BR60J226ME39</td>
</tr>
<tr>
<td>D₁</td>
<td>V_F = 0.35 V</td>
<td>I_R = 7 µA @ 25°C</td>
<td>SOD323</td>
<td>PMEG2005EJ</td>
</tr>
<tr>
<td>L₁</td>
<td>15 µH</td>
<td>DCR = 260 mΩ</td>
<td>4 x 4 x 1.8 mm</td>
<td>LPS4018-153MLC</td>
</tr>
<tr>
<td>R₁</td>
<td>1 kΩ</td>
<td></td>
<td>0603</td>
<td></td>
</tr>
</tbody>
</table>

2.1 The Inductor

The LPS series of inductor coils, from Coilcraft, have low DC resistance (DCR) and low core loss. They are shielded and available in relatively small packages. A large number of package options are also available.

DCR depends on the type and make of inductor. As an example, the DCR of some inductor coils are summarized in Table 2-2 below. The lower the DCR the better the efficiency of the boost regulator.

Table 2-2. Maximum DCR of Some Inductor Coils (Manufacturer’s Data).

<table>
<thead>
<tr>
<th>Inductor</th>
<th>DCR</th>
<th>Inductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPS3314-153MLC</td>
<td>440 mΩ</td>
<td>15 µH</td>
</tr>
<tr>
<td>LPS4018-153MLC</td>
<td>260 mΩ</td>
<td>15 µH</td>
</tr>
<tr>
<td>LPS6235-153MLC</td>
<td>125 mΩ</td>
<td>15 µH</td>
</tr>
</tbody>
</table>

Figure 2-1 below illustrates how booster efficiency varies with type of inductor and, consequently, DCR. Component values used are those listed in Table 2-1.

Figure 2-1. Booster Efficiency versus Type of Inductor at V_BAT = 1.2V and T = 25°C.
Core losses are device specific and are given by coil manufacturers. The lower the core loss the better the efficiency of the boost regulator.

As a rule of thumb, core loss is of importance at low load currents and DCR is of importance at large load currents.

2.2 The Diode

Schottky diodes have low forward voltages ($V_F$) but relatively high reverse leakage currents ($I_R$).

Before making a diode selection it is important to know the operating temperature range of the design since forward voltage and reverse leakage current are highly temperature dependent variables. Typically, design dependent trade-offs between $V_F$ and $I_R$ need to be made. For this purpose it is vital to understand how the two parameters affect boost operation, as follows:

- The forward voltage of the diode affects the efficiency at high loads and load currents. The lower the forward voltage the better the efficiency at high currents
- The reverse leakage current affects the Active Low Current Mode of operation and operation at light loads. The lower the reverse leakage current the better the efficiency at low currents

It should be noted that the trade-offs made at room temperature do not necessarily hold at other temperatures. Figure 2-2 below illustrates how booster efficiency depends on temperature. All component values are listed in Table 2-1.

Figure 2-2. Booster Efficiency versus Diode Temperature at $V_{BAT} = 1.2V$.

![Booster Efficiency versus Diode Temperature at $V_{BAT} = 1.2V$.](image)

The temperature dependency of $V_F$ and $I_R$ are particular to the make and model of diode used. Figure 2-3 below illustrates how booster efficiency at high temperatures is affected by the type of diode used. Component values (excluding the diodes) are those listed in Table 2-1.
Table 2-3 below shows typical average currents drawn from the battery with two types of diodes and in two operating conditions. In both cases, Power-down Mode with Watchdog Timer disabled and enabled, the boost converter stays in Active Low Current Mode (LCM). Component values (excluding the diodes) are those listed in Table 2-1.

Table 2-3. Typical Average Current Drawn from a Battery in the LCM Mode.

<table>
<thead>
<tr>
<th></th>
<th>BAT20J (IR = 0.75 µA)</th>
<th>PMEG2005EJ (IR = 7.5 µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-down Mode, Watchdog Timer disabled</td>
<td>2.7 µA</td>
<td>15 µA</td>
</tr>
<tr>
<td>Power-down Mode, Watchdog Timer enabled</td>
<td>16 µA</td>
<td>28 µA</td>
</tr>
</tbody>
</table>

Table 2-4 below shows typical average currents drawn from the battery with two types of diodes and five different loading conditions. In all these cases the boost converter stays in Active Regulated Mode.

Table 2-4. Typical Average Current Drawn from a Battery in the Regulated Mode.

<table>
<thead>
<tr>
<th></th>
<th>BAT20J (IR = 0.75 µA)</th>
<th>PMEG2005EJ (IR = 7.5 µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC = 1 mA, Loading Current drawn from VCC</td>
<td>3.2 mA</td>
<td>3.2 mA</td>
</tr>
<tr>
<td>ICC = 5 mA</td>
<td>15 mA</td>
<td>15 mA</td>
</tr>
<tr>
<td>ICC = 10 mA</td>
<td>32 mA</td>
<td>31 mA</td>
</tr>
<tr>
<td>ICC = 20 mA</td>
<td>66 mA</td>
<td>64 mA</td>
</tr>
<tr>
<td>ICC = 30 mA</td>
<td>100 mA</td>
<td>97 mA</td>
</tr>
</tbody>
</table>

Total average current ($I_{in,tot}$) drawn from the battery in an application can be calculated with the equation below when the average times ($t_x$) of the different loading conditions and their input currents ($I_{in,x}$), respectively, are known.

$$I_{in,tot} = \frac{\sum (t_x \cdot I_{in,x})}{\sum t_x}$$
3 PCB Layout

Good component placement is important for proper regulator functionality. Following are some guidelines, listed in order of importance:

1. One layer of PCB should be reserved for ground, only. Extended ground areas and vias should have as high conductance as possible.

2. The wires of the LSW node (between LSW pin, inductor L₁ and diode D₁) should be as wide as possible but the area of the node as small as possible. The diode should be close to the inductor.

3. Output capacitor C₃ should be as close to diode D₁ as possible. Similarly, capacitor C₃ (and C₄, if implemented) should be as close to supply (V_{CC}) and ground (GND) pins as possible.

4. Input Capacitor C₁ should be placed as close to inductor L₁ as possible. Also, the tracks from the battery to the input capacitor should be as short as possible. The track going to the battery should have a high conductance because of high current.

5. The capacitor of low-pass-filter (R₁-C₂ in Figure 1-1) should be located as close to the V_{BAT} and GND pins as possible.

PCB tracks should have a high conductance, especially those carrying high current. Table 3-1 below summarizes the high current paths in the design. See Figure 3-1 and Figure 3-2 for recommended track layouts.

<table>
<thead>
<tr>
<th>Current Path</th>
<th>Description</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery(+) – ( V_{IN} ) – L₁ – LSW Pin</td>
<td>Current flow from battery to device during ON time of switching cycle</td>
<td>Current flows here for about 70% of the time</td>
</tr>
<tr>
<td>GND Pin – Ground Layer – Battery(-)</td>
<td>Return current to battery during ON time of switching cycle</td>
<td></td>
</tr>
<tr>
<td>Battery(+) – ( V_{IN} ) – L₁ – D₁ – C₃</td>
<td>Current flow from battery during OFF time of switching cycle</td>
<td>Current flows here for about 30% of the time</td>
</tr>
<tr>
<td>C₃ – Ground Layer – Battery(-)</td>
<td>Return current to battery via ground layer during OFF time of switching cycle</td>
<td></td>
</tr>
</tbody>
</table>

3.1 SOIC Package

Figure 3-1 below shows an example of the top layer in a design using the ATtiny43U in SOIC package. Component values can be found in Table 2-1.
Figure 3-1. Component Layout Recommendation for SOIC package.

In addition to the top layer, it is also recommended to include a separate ground layer and bolt the ground areas of the top layer to the ground layer firmly by several vias. Ground fillings in the top layer are to be avoided since they are prone to pick up noise.
3.2 MLF Package

Figure 3-2 below shows an example of the top layer in a design using the ATtiny43U in MLF package. Component values can be found in Table 2-1.

Figure 3-2. Component Layout Recommendation for MLF package.

In addition to the top layer, it is also recommended to include a separate ground layer and bolt the ground areas of the top layer to the ground layer firmly by several vias. The exposed die pad of the MLF package should be connected to the ground layer through via matrices. Ground fillings in the top layer are to be avoided since they are prone to pick up noise.
3.3 Minimum Layout

Figure 3-3 below shows a proven example of minimum layout, that can be used with certain trade-offs of specifications. The layout is made for the smallest components available, and narrow wire widths and spacing on PCB.

Figure 3-3. Dedicated Minimum Layout.

The spacing between components in this layout is 1 mm in minimum. Depending on the selected component mounting process the spacing can be adjusted accordingly. The line widths are 0.3 mm in the power path (V\text{IN}, LSW, V\text{CC} and GND wires). The line thickness should be selected so that the wires can sustain RMS currents of up to 250 mA.

The new EPL and XPL inductor series from Coilcraft utilize very small packages, but they are available only with inductance values of up to 10 µH. However, the ATtiny43U can be used with a 10 µH (±20%) inductor with certain limitations. The lower inductance value causes the current to ramp up faster and higher than with the nominal 15 µH inductor, causing higher losses in the power path. Due to these losses, the temperature of the components and wires increases few degrees (C) with full load.
The components for this minimum layout and its tighter specifications are shown in the Table 3-2 below.

### Table 3-2. Components and Specification Limitations for the Minimum Layout.

<table>
<thead>
<tr>
<th>Comp.</th>
<th>Value</th>
<th>Note</th>
<th>Package</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>4.7 µF</td>
<td></td>
<td>0402</td>
<td>GRM155R60G475ME</td>
</tr>
<tr>
<td>C2</td>
<td>22 nF</td>
<td></td>
<td>0201</td>
<td>GRM033R60J223KE01D</td>
</tr>
<tr>
<td>C3</td>
<td>22 µF</td>
<td></td>
<td>0805</td>
<td>GRM21BR60J226ME39</td>
</tr>
<tr>
<td>D1</td>
<td>V_F = 0.45 V</td>
<td>I_R = 2 µA @ 25°C</td>
<td>SOD882</td>
<td>PMEG2005EL</td>
</tr>
<tr>
<td>L1</td>
<td>10 µH</td>
<td>DCR = 460 mΩ</td>
<td>2 x 2 x 1.4 mm</td>
<td>EPL2014-103MLC</td>
</tr>
<tr>
<td>R1</td>
<td>1 kΩ</td>
<td></td>
<td>0201</td>
<td>RC0201JR-071KL</td>
</tr>
</tbody>
</table>

Maximum Load Current: $I_{LOAD\ (Max)} = 20\ mA$

Maximum Input Voltage: $V_{BAT\ (Max)} = 1.6\ V$

With this layout the physical size is reduced to minimum, but the specification limits and the efficiency of the converter are somewhat reduced.
4 Smoothing the Supply Voltage

High-frequency voltage spikes appear in supply voltage ($V_{CC}$) at moments when the inductor is switched on and off, as illustrated in Figure 4-1 below. Low-frequency voltage variation between spikes is referred to as ripple.

![Figure 4-1. Typical Voltage Spikes and Ripple at $V_{CC}$](image)

Supply voltage ripple and spikes do not affect the operation of the boost regulator but may be undesired in some applications.

The amplitude of $V_{CC}$ ripple mainly depends on the following factors:

- Magnitude of load current. The larger the load current the larger the voltage ripple
- Size and number of output capacitors. Voltage ripples can typically be kept reasonable by using a combination of large and small capacitors
- Quality of output capacitors. Low ESR reduces voltage ripple

The amplitude of $V_{CC}$ spikes depends on the following factors:

- Actual PCB layout. Poor layout and long tracks increases spike magnitudes and may introduce longer periods of ringing. Output capacitors should be placed as close as possible to the $V_{CC}$ pin
- Quality of output capacitors. Low ESL reduces spikes

Table 4-1 below shows typical voltage ripple that can be expected. Please note that actual voltage ripple is highly application dependent and does vary.

<table>
<thead>
<tr>
<th>Load Current</th>
<th>$V_{CC}$ Filter Capacitors</th>
<th>Typical $V_{P-P}$ Spikes</th>
<th>Typical $V_{P-P}$ Ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5 mA</td>
<td>100 nF</td>
<td></td>
<td>22 μF</td>
</tr>
<tr>
<td></td>
<td>22 nF</td>
<td></td>
<td>47 μF</td>
</tr>
<tr>
<td></td>
<td>100 nF</td>
<td></td>
<td>22 μF</td>
</tr>
<tr>
<td></td>
<td>22 nF</td>
<td></td>
<td>22 μF</td>
</tr>
<tr>
<td></td>
<td>4.7 nF</td>
<td></td>
<td>22 μF</td>
</tr>
<tr>
<td>30 mA</td>
<td>22 μF</td>
<td>100 mV</td>
<td>40 mV</td>
</tr>
</tbody>
</table>
5 Start Circuit for Low Voltages

The minimum operating voltage of the boost converter is lower than the start voltage. During normal operation battery charge will drop and, as a result, so will battery voltage. When battery voltage has dropped below boost start voltage a disruption of supply voltage may leave the application in a state where battery voltage is too low for the boost converter to start. Disruptions in supply voltage are unwanted but may occur when, for example, the battery driven application is accidentally dropped.

It is possible to recover and continue operation in situations where battery voltage has already been depleted below boost converter start level. One method for recovery is to implement a low voltage start button, as illustrated in Figure 5-1 below. The actual start circuit is outlined with a dotted line.

Figure 5-1. Schematic of Boost Converter Circuit with Low Voltage Start.

When button, S1, is pushed the supply voltage is momentarily raised to a level above start voltage, allowing the boost converter to start.

5.1 Operation

When a battery is applied to VIN all capacitors start to charge and voltage at VBAT quickly ramps up to the battery voltage level. After capacitors have charged, and assuming C1 = CS1, pushing button S1 connects the two capacitors in series, briefly doubling the voltage at VBAT and helping the boost converter to start.
After reaching its maximum the voltage at \( V_{\text{BAT}} \) starts to drop, as illustrated in Figure 5-2 below.

**Figure 5-2.** Typical Start Pulse at \( V_{\text{BAT}} \), Generated when \( S_1 \) Pressed.

For the low voltage start circuitry to be successful the voltage at \( V_{\text{BAT}} \) needs to remain above the start level \( V_{\text{START}} \) sufficiently long. The time required, \( t_p \), depends on the battery voltage and the peak amplitude. Typical values are summarized in Table 5-1 below. The values given assume a worst-case start voltage of 1.35V. Actual values may be lower.

<table>
<thead>
<tr>
<th>Battery Voltage, ( V_{\text{IN}} )</th>
<th>Pulse Width, ( t_p )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7 V</td>
<td>5 ms</td>
</tr>
<tr>
<td>0.8 V</td>
<td>3 ms</td>
</tr>
<tr>
<td>0.9 V</td>
<td>1 ms</td>
</tr>
<tr>
<td>1.0 V</td>
<td>0.1 ms</td>
</tr>
</tbody>
</table>

Switch \( S_W \) provides the means for preventing the design from draining the battery during long shell times. In its simplest form this can be a piece of isolating tape between the battery pole and the connector, and simply pulled away when the design is taken into use.

### 5.2 Component Values

Component values given in Table 5-2 result in a start pulse that is above 1.35V for at least 0.3ms, provided battery voltage is at least 1V. This is sufficient for starting the boost converter.

The start pulse can be prolonged by increasing \( R_1 \) but care should be taken to keep the low-pass filter \( R_1-C_2 \) within limits. Also, when using the ADC to measure battery voltage the size of \( R_1 \) needs to be observed. See device data sheet for more details.

Pulse width can be increased also by increasing the size of \( C_{51} \).
Table 5-2. Typical Component Values for $V_{IN} \geq 1V$.

<table>
<thead>
<tr>
<th>Component</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$, $C_{S1}$</td>
<td>2.2 µF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>100 nF</td>
</tr>
<tr>
<td>$C_3$</td>
<td></td>
</tr>
<tr>
<td>$C_4$</td>
<td>Not critical</td>
</tr>
<tr>
<td>$D_1$</td>
<td></td>
</tr>
<tr>
<td>$L_1$</td>
<td></td>
</tr>
<tr>
<td>$R_1$</td>
<td>680 Ω</td>
</tr>
<tr>
<td>$R_{S1}$</td>
<td>100 kΩ</td>
</tr>
</tbody>
</table>
6 Bypassing Hardware Shutdown

It is possible to configure the boost converter such that it does not enter Stop Mode when battery voltage drops below shutdown voltage. This allows the design to drain the battery cell completely. This procedure is recommended for non-rechargeable batteries, only. It should be noted, that draining the battery is harmful for most rechargeable battery chemistries.

Hardware shutdown of boost converter is bypassed by connecting \( V_{\text{BAT}} \) to a voltage source that does not drop below shutdown voltage. The most obvious choice is to short \( V_{\text{BAT}} \) to \( V_{\text{CC}} \), as shown in Figure 6-1 below. This connection allows enough voltage from \( V_{\text{IN}} \) to \( V_{\text{BAT}} \) for the boost converter to start and keeps \( V_{\text{BAT}} \) as high as possible once the converter is up and running. In this mode of operation the boost regulator can not be stopped by firmware.

Figure 6-1. Schematic for Battery Drain Configuration.

When battery is drained the boost converter input voltage drops and the efficiency of the converter decreases. This means that at lower input voltages more input current is required to generate the same load current. It also means that at lower voltages the maximum load current the boost converter can provide decreases. This is illustrated in Table 6-1 below, where \( I_{\text{LOAD}} \) is the maximum current the boost converter can provide while still maintaining regulation.

Table 6-1. Typical Supply and Load Currents with Hardware Control Bypassed.

<table>
<thead>
<tr>
<th>Input Voltage, ( V_{\text{IN}} )</th>
<th>Load Current, ( I_{\text{LOAD}} ) ( ^{(1)} )</th>
<th>Input Current, ( I_{\text{IN}} ) ( ^{(2)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6 V</td>
<td>11 mA</td>
<td>80 mA</td>
</tr>
<tr>
<td>0.5 V</td>
<td>8 mA</td>
<td>70 mA</td>
</tr>
<tr>
<td>0.4 V</td>
<td>5 mA</td>
<td>60 mA</td>
</tr>
<tr>
<td>0.3 V</td>
<td>2.5 mA</td>
<td>45 mA</td>
</tr>
<tr>
<td>0.2 V</td>
<td>1 mA</td>
<td>30 mA</td>
</tr>
</tbody>
</table>

Notes:  
1. Max current the converter can provide while maintaining regulation \( (V_{\text{CC}} > 2.7V) \)  
2. Current drawn from source at given load current
7 Low Voltage Design with Turn-Off Switch

This design combines the previously described low voltage and battery drain techniques. It also includes a two-pole, two-position switch, which allows the design to be completely turned off, thus extending battery life. The design is illustrated in Figure 7-1, below. Component values are listed in Table 7-1.

Figure 7-1. Schematic for Low Voltage and Battery Drain Configuration.

Table 7-1. Component Values.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>4.7 µF</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>22 µF</td>
<td></td>
</tr>
<tr>
<td>C_{S1}</td>
<td>1 µF</td>
<td></td>
</tr>
<tr>
<td>C_{S2}</td>
<td>0.47 µF</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>(not critical)</td>
<td>See page 3 for design guidelines</td>
</tr>
<tr>
<td>L1</td>
<td>(not critical)</td>
<td>See page 2 for design guidelines</td>
</tr>
<tr>
<td>R_{S1}</td>
<td>220 kΩ</td>
<td></td>
</tr>
<tr>
<td>R_{S2}</td>
<td>470 kΩ</td>
<td></td>
</tr>
<tr>
<td>R_{S3}</td>
<td>22 kΩ</td>
<td></td>
</tr>
<tr>
<td>T1</td>
<td>BC847C</td>
<td>NPN</td>
</tr>
</tbody>
</table>
8 Typical Component Values

A typical use of the boost converter is illustrated in Figure 1-1, on page 1. Components can be optimized depending on the type of application, as discussed in section Component Optimization, on page 2. The Table 8-1 below presents recommendations for three types of applications (with emphasis on high performance, optimized area and cost effective). All values are guidelines, only. Components with similar specifications from other manufacturers can be used also.

Table 8-1. Typical Component Values vs. Design Emphasis.

<table>
<thead>
<tr>
<th>Part</th>
<th>Design Emphasis</th>
<th>High Performance</th>
<th>Small Area</th>
<th>Low Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>High Performance</td>
<td>GRM219R60J475KE19 (1)</td>
<td>GRM155R60G475ME (2)</td>
<td>≥ 2 µF</td>
</tr>
<tr>
<td>C2</td>
<td>Small Area</td>
<td>100 nF</td>
<td>100 nF (2)</td>
<td>_ (3)</td>
</tr>
<tr>
<td>C3</td>
<td>Low Cost</td>
<td>GRM21BR60J226ME39 (1)</td>
<td>GRM21BR60J226ME39 (1)</td>
<td>≥ 20 µF</td>
</tr>
<tr>
<td>C4</td>
<td></td>
<td>100 nF</td>
<td>_ (4)</td>
<td>_ (4)</td>
</tr>
<tr>
<td>D1</td>
<td>High Performance</td>
<td>PMEG2005EJ (5)</td>
<td>PMEG2005EL (6)</td>
<td>I_{RMS} (Max) ≥ 0.5 A</td>
</tr>
<tr>
<td>L1</td>
<td></td>
<td>LPS4018-153MLC</td>
<td>LPS3314-153MLC</td>
<td>I_{RMS} (Max) ≥ 0.5 A</td>
</tr>
<tr>
<td>R1</td>
<td></td>
<td>1 kΩ</td>
<td>1 kΩ (2)</td>
<td>_ (3)</td>
</tr>
</tbody>
</table>

Notes: 1. Package: 0805
2. Package: 0402
3. Increases voltage ripple at VBAT pin.
4. Not required, if MLF packaged device used.
5. Use BAT20J for very low input currents in LCM mode, see Table 2-3 on page 4.
6. Package: SOD882
9 Firmware Example

The assembly code below illustrates how to use the ADC to monitor the battery voltage and shut down the boost regulator when voltage drops below a given threshold. The code example is written for AVR Studio Assembler.

```
;***************************************************************************
; Program: ATtiny43U_ADC_STOP_example
; $Date: 2010/06/01 12:00:00 $
; $Revision: 1.2 $
;***************************************************************************

.include "tn43Udef.inc"

.def temp =r16 ; Temporary registers
.def temp2 =r17
.def tempL =r18 ; Temporary ADC low byte
.def tempH =r19 ; Temporary ADC high byte
.def accL =r20 ; Accumulator low byte
.def accH =r21 ; Accumulator high byte

rjmp RESET ; Reset Handler

.org 0x0080

RESET:
  ldi temp, 0x5f ; Set stack pointer
  ldi temp2, 0x01
  out SPL, temp
  out SPH, temp2
  rjmp ADC_VBAT

ADC_VBAT:
  ldi temp, 0b01000110 ; Int 1.1V Ref and VBAT
  out ADMUX, temp
  ldi temp, 0b10000011 ; Enable ADC and prescaler mclk/8 1MHz
  out ADCSRA, temp
  ldi temp, 0b00000000 ; ADLAR bit cleared
  out ADCSRB, temp

ADC_start:
  ldi accL, 0x00 ; Clear accumulator accH:accL
  ldi accH, 0x00
```
rcall Make_conversion ; Make 1'st conversion
add accL, tempL
adc accH, tempH
rcall Make_conversion ; Make 2'nd conversion
add accL, tempL
adc accH, tempH
rcall Make_conversion ; Make 3'rd conversion
add accL, tempL
adc accH, tempH
rcall Make_conversion ; Make 4'th conversion
add accL, tempL
adc accH, tempH
lsr accH   ; Divide result by 4
ror accL
lsr accH
ror accL   ; 10-bit average result in registers accH:accL

lsr accH   ; Skip 2 LSB bits from 10-bit average
ror accL
lsr accH
ror accL   ; 8-bit result in register accL

; Use internal 1.1V (typical) reference to check if VBAT is below
; 8-bit stop level
; 0x74 ~ 1.0V
; 0x68 ~ 0.9V
; 0x5d ~ 0.8V

cpi accL, 0x68  ; If VBAT < 0.9V,
brlo Stop_boost ; then stop boost

rjmp ADC_start

Make_conversion:
sbi ADCSRA, ADSC
Wait_conversion_ready:
sbic ADCSRA, ADSC
rjmp Wait_conversion_ready
in tempL, ADCL
in tempH, ADCH
ret
Stop_boost:
  ldi temp, 0x00 ; Disable all outputs
  out DDRA, temp
  out DDRB, temp

  ldi temp, 0b01000000 ; 1.1Vref and ADC0
  out ADMUX, temp
  ldi temp, 0b00000000 ; Disable ADC
  out ADCSRA, temp

; Boost stop sequence
  ldi temp, 0b11000000
  out PRR, temp
  ldi temp, 0b10000000
  out PRR, temp
  ldi temp, 0b01000000
  out PRR, temp
  rjmp Read_Boost_Status

Read_Boost_Status: ; Poll boost status bit.
  sbis ADCSRB, 7 ; Jump to reset if boost is restarted
  rjmp Read_Boost_Status ; before mcu core POR or BOD reset
  rjmp RESET
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