AT73C240 - Audio Power Amplifier Filtering and Gain

Power Management and Analog Companions (PMAAC)

Application Note

1. Scope

This document decribes how to determine the capacitance of the Input Capacitors of the Audio Power Amplifier for the product AT73C240.

AT73C240 has an Audio Power Amplifier, bridge-tied loaded, designed in CMOS technology, capable of driving an 8 Ohm Loudspeaker, making it suitable as a hands-free speaker driver in Wireless Handset Application.

High quality mono output is provided. The DAC output can be connected trough a buffer stage to the input of the Audio Power Amplifier, using two coupling capacitors.

This document defines how to calculate the required capacitance of these two coupling capacitors.

Caution: the Audio power amplifier is not internally protected against short-circuit. The user should avoid any short-circuit on the load.

2. Operating Conditions

Table 2-1. Operating Condition Table For AT73C240 Product

Parameter/Function	Pads	Min	Max	Unit
Storage Temperature	--	-55	150	°C
Operating Temperature	--	-40	85	°C
Audio Power Input Voltage	VBAT	3.0	5.5	V
Digital Input Voltage	VDIG	2.4	3.3	V
Analog Input Voltage	AVDD, AVDDHS	2.7	3.3	V

3. Glossary

BW -- Bandwith

CMRR -- Common Mode Rejection Ratio

DAC -- Digital to Analog Converter

PA -- Audio Power Amplifier

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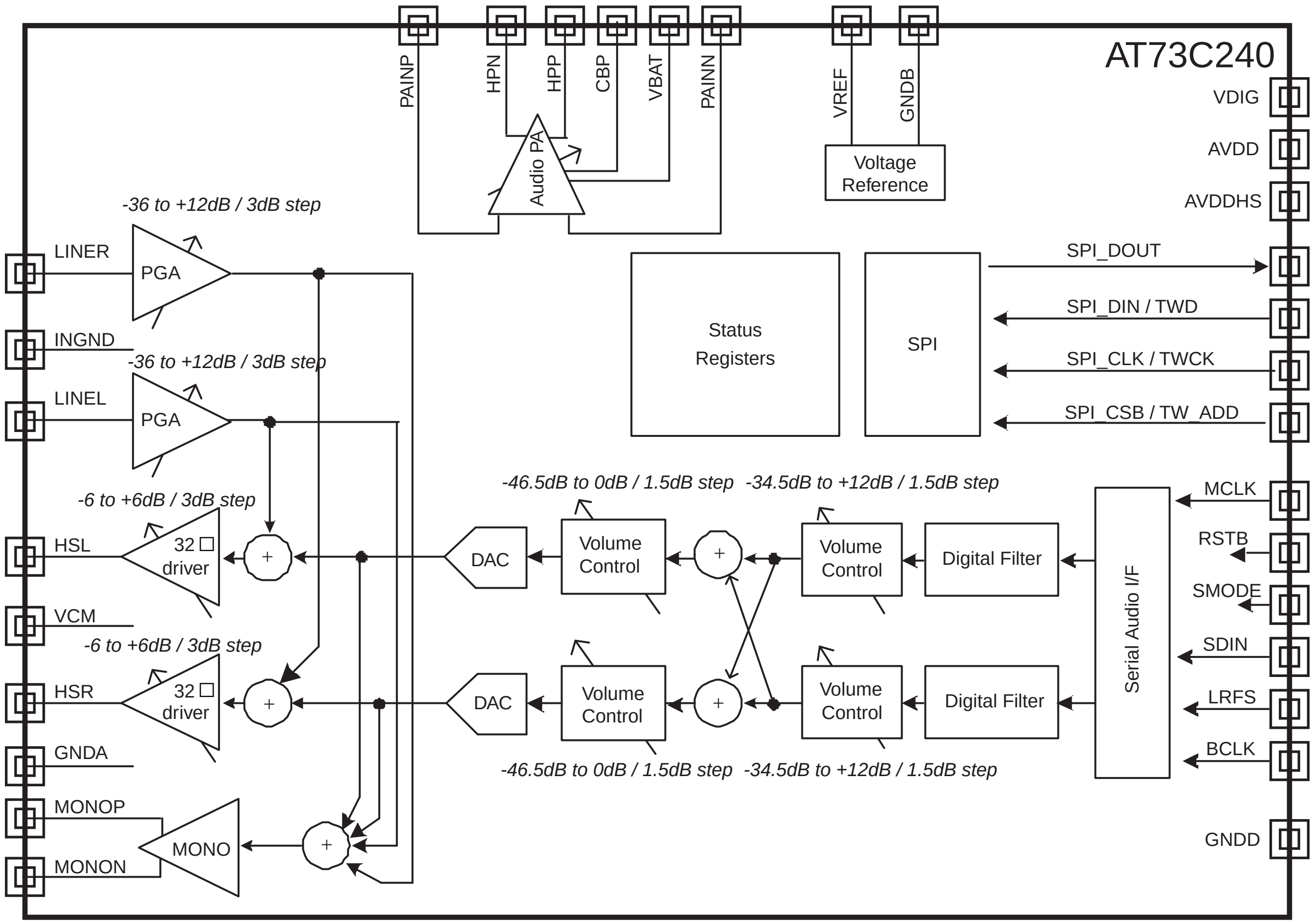
4. AT73C240 Block Diagram

Figure 4-1. AT73C240 Block Diagram



5. Power Amplifier Inupt Capacitor Selection

5.1 Use Needs

The two input capacitors, C8 and C15 in Figure 5-1, connected between MONON-PAINN and MONOP-PAINP, affect two parameters:

- The low frequency cut-off
- The common mode rejection at low frequencies.

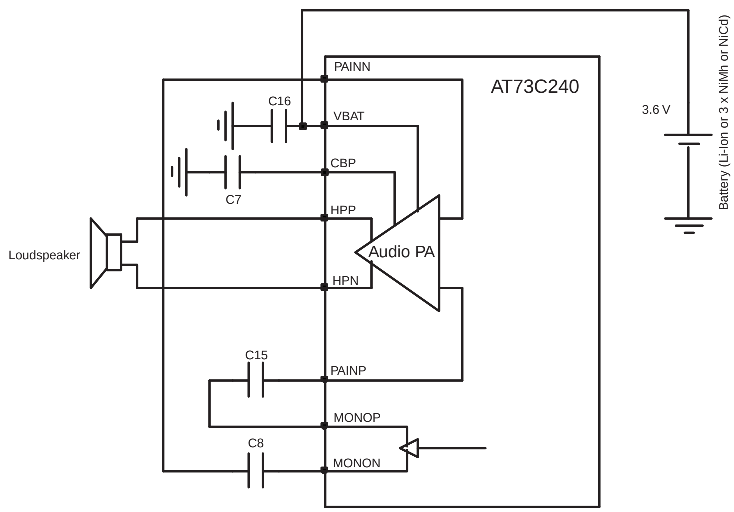
The low frequency cut-off depends on those capacitor values and the PA input impedance.

This impedance also depends on the gain selected (the higher the gain, the lower the input impedance).

The low frequency cut-off is generally chosen to allow full bandwidth reproduction in all cases. The worst case is the highest low frequency cut-off available.

5.2 Power Amplifier Apllication Diagram

Figure 5-1. AT73C240 Power Amplifier Application Diagram



5.3 Calculation

Since minimum input impedance value is 10kOhms at maximum gain, the input capacitance regarding the lower frequency to reproduce (Fcl) is calculated at follows:

$$Cin = 10^5 / (6283 \times Fcl)$$

- Fcl is expressed in Hz
- Cin is expressed in µF

For a 50Hz low frequency cut-off, the calculated value is 0.318µF, or a 330nF as a standard capacitor value.

Another parameter is the CMRR: to ensure a 40dB minimum rejection at low frequency, the matching between the two input capacitors must be better than 1%.

6. Power Amplifier Input Impedance Versus Gain

The input impedance depends on the power amplifier gain. The minimum input impedance (15kOhms typ, 10kOhms min) occurs with maximum gain value selected (+20dB), and at the opposite the maximum input impedance (150kOhms typ, 100kOhms min) is obtained with the minimum gain value (-22dB).

The following table gives all typical process input impedance values versus the gain selected.

Table 6-1. Input Impedance vs Power Amplifier Gain

Input Impedance (Ohms)	Gain (dB)	Input Impedance (Ohms)	Gain (dB)
15k	+20	100k	-4
20k	+17	113k	-7
27k	+14	124k	-10
36k	+11	133k	-13
46k	+8	140k	-16
59k	+5	145k	-19
71k	+2	150k	-22
86k	-1		

Revision History

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