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Section 1

Introduction

Congratulations on your purchase of the AT73C260-EK1. It is designed to give designers a quick start to evaluate the Interchip USB Transceiver capability of the AT73C260 and for prototyping and testing of new designs.

1.1 Scope

This document describes the AT73C260-EK1. This board is designed to allow an easy evaluation of the functionalities and the various interchip configuration modes.

To increase its capabilities for demonstration, this standalone board has several configuration modes according the interconnection between host and device.

This User Guide acts as a general getting started guide as well as a complete technical reference for advanced users.

This document refers the AT73C260 Datasheet.

Typical Applications:

- Mobile USB UICC (ETSI 102 600)
- PC USB UICC
- Token USB
1.2 AT73C260-EK1 Features

The AT73C260-EK1 provides the following features:

- **Power Supply:**
  - VBUS Connector for Host Connection

- **On-board resources:**
  - USB Connector Type A,
  - USB Connector Type B,
  - 2 Micro USB Connector Type AB,
  - UICC Interface Connector,
  - Smart Card Reader Connector,
  - Connector for FPGA interconnection.

- **On-board jumpers:**
  - Jumpers for M<2:0> pads, in order to configure the modes of interchip connection,
  - Jumpers for PVRF configuration,
  - Jumpers for set of the pull-down resistors on PDP, PDM,
  - Jumpers for UICC Connector configuration,
  - Jumpers for load connection on power supplies.

1.3 Deliverables

The AT73C260-EK1 package contains the following items:

- An AT73C260-EK1 board,
- One CD-ROM containing the AT73C260-EK1 User Guide and a full AT73C260 Datasheet.
**Figure 1-1.** AT73C260-EK1 Top View (card photo)

The AT73C260 is located in the center of the AT73C260-EK1 on the Components Side.

**Figure 1-2.** AT73C260-EK1 Card With Available Connections
Figure 1-3. AT73C260-EK1 Components Side
Section 2
Getting Started

2.1 Jumper Electrostatic Warning

The AT73C260-EK1 evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be connected when handling the board. Avoid touching the components pins or any metallic element.

2.2 Requirements

In order to set up the AT73C260-EK1 evaluation kit the following items are needed:

1. The AT73C260-EK1 evaluation board itself.
2. One or more of the following connections:
   - USB Type A Cable, USB Type B Cable, Micro USB Type AB Cable
   - FPGA Cable, UICC Connector
3. Input/Output devices for upstream and downstream connection.

2.3 Instructions

2.3.1 To start the AT73C260-EK1 board

Configure the on-board jumpers as in the relevant paragraph below and connect the dedicated connections:

1. Digital 6 Wires DAT_SE0 to IC_USB1.0: Section 2.6.1 "Mode PHY_6_SE0" on page 2-14
2. Digital 4 Wires DAT_SE0 to IC_USB1.0: Section 2.6.2 "Mode PHY_4_SE0" on page 2-15
3. Digital 6 Wires DP_DM to IC_USB1.0: Section 2.6.3 "Mode PHY_6_DPDM" on page 2-16
4. Digital 4 Wires DP_DM to IC_USB1.0: Section 2.6.4 "Mode PHY_4_DPDM" on page 2-17
5. Digital 3 Wires ULPI to IC_USB1.0: Section 2.6.5 "Mode PHY_3_ULPI" on page 2-18
6. USB2.0 Section 7 to IC_USB1.0: Section 2.6.6 "Mode S7_ICC" on page 2-19
7. PC USB2.0 Section 7 to IC_USB1.0 with VCC driven by DBB: Section 2.6.7 "Mode S7_ICC_BB" on page 2-20
8. USB2.0 Section 7 to IC_USB1.0 with VCC fixed by PVRF: Section 2.6.8 "Mode S7_ICC_TK" on page 2-21
9. IC_USB1.0 to USB2.0 Section 7: Section 2.6.9 "Mode ICC_S7" on page 2-22
10. Voltage Class Converter: Section 2.6.10 "Mode VCC" on page 2-23
2.3.2 To turn off the AT73C260-EK1 evaluation board

- Release all the connections made between Host/Device and AT73C260-EK1 Evaluation Kit

2.4 Block Diagram

Figure 2-1. AT73C260 Block Diagram
2.5 Typical Application Connections

Figure 2-2. Application Connections: Mode PHY_6_SEO

Hardware Setup Example:

- $V_{HCC}$ is forced at 3.3V. (Voltage Range: $1.65V < V_{HCC} < 3.6V$)
- $V_{PVCC}$ is forced at 3.0V. (Voltage Range: $1.65V < V_{PVCC} < 3.6V$)
Figure 2-3. Application Connections: Mode PHY_4_SEO

Hardware Setup Example:
- HVCC is forced at 3.3V. (Voltage Range: 1.65V < HVCC < 3.6V)
- PVCC is forced at 3.0V. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-4. Application Connections: Mode PHY_6_DPDM

Hardware Setup Example:
- $H_{VCC}$ is forced at 3.3V. (Voltage Range: $1.65V < H_{VCC} < 3.6V$)
- $P_{VCC}$ is forced at 3.0V. (Voltage Range: $1.65V < P_{VCC} < 3.6V$)
Figure 2-5. Application Connections: Mode PHY_4_DPDM

Hardware Setup Example:
- HVCC is forced at 3.3V. (Voltage Range: 1.65V < HVCC < 3.6V)
- PVCC is forced at 3.0V. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-6. Application Connections: Mode PHY_3_ULPI

Hardware Setup Example:

- HVCC is forced at 3.3V. (Voltage Range: 1.65V < HVCC < 3.6V)
- PVCC is forced at 3.0V. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-7. Application Connections: Mode S7_ICC

 Hardware Setup Example:

- $H_{VCC}$ is forced at 3.3V. (Voltage Range: $1.65V < H_{VCC} < 3.6V$)
- $P_{VCC}$ is forced at 3.0V. (Voltage Range: $1.65V < P_{VCC} < 3.6V$)
Figure 2-8. Application Connections: Mode S7_ICC_BB

Hardware Setup Example:
- HVCC is fixed at 3.3V. It is supplied by VBUS.
- PVCC is fixed and controlled by PVRF delivered by Digital Base Band Chip. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-9. Application Connections: Mode S7_ICC_TK

Hardware Setup Example:
- HVCC is fixed at 3.3V. It is supplied by VBUS.
- PVCC is fixed by external resistor ratio R4/R5 on PVRF. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-10. Application Connections: Mode ICC_S7

Hardware Setup Example:

- HVCC is forced at 3.3V. (Voltage Range: 1.65V < HVCC < 3.6V)
- PVCC is forced at 3.3V. (Voltage Range: 1.65V < PVCC < 3.6V)
Figure 2-11. Application Connections: Mode VCC

Hardware Setup Example:
- HVCC is forced at 3.3V. (Voltage Range: 1.65V < HVCC < 3.6V)
- PVCC is forced at 3.0V. (Voltage Range: 1.65V < PVCC < 3.6V)
2.6 Switch and Jumpers configuration according Interchip Mode

The AT73C260-EK1 can be used for various interchip configurations. These modes and the configuration to achieve in order to operate in this mode are described below. The following configuration modes are described:

- Digital 6 Wires unidirectional DAT_SE0 to IC_USB1.0: “Mode PHY_6_SE0” on page 2-14
- Digital 4 Wires bidirectional DAT_SE0 to IC_USB1.0: “Mode PHY_4_SE0” on page 2-15
- Digital 6 Wires unidirectional DP_DM to IC_USB1.0: “Mode PHY_6_DPDM” on page 2-16
- Digital 4 Wires bidirectional DP_DM to IC_USB1.0: “Mode PHY_4_DPDM” on page 2-17
- Digital 3 Wires bidirectional ULPI to IC_USB1.0: “Mode PHY_3_ULPI” on page 2-18
- USB2.0 Section 7 to IC_USB1.0: “Mode S7_ICC” on page 2-19
- PC’s USB2.0 Section 7 to IC_USB1.0 with VCC driven by DBB: “Mode S7_ICC_BB” on page 2-20
- USB2.0 Section 7 to IC_USB1.0 with VCC fixed by PVRF: “Mode S7_ICC_TK” on page 2-21
- IC_USB1.0 to USB2.0 Section 7: “Mode ICC_S7” on page 2-22
- Voltage Class Converter: “Mode VCC” on page 2-23
2.6.1 Mode PHY_6_SE0

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force M<2:0> pins to ground by switching SW1, SW2 and SW3 to ground.
- Connect HOST FPGA connector on J24.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.

Three devices choices are possibles:
- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed Jumpers as follows:
- Close Jumper J25
- Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-12. On Board Jumpers, Switches and Connectors Description
2.6.2 Mode PHY_4_SE0

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 \(\Omega\) resistor on R8. J11 Jumper must be opened.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force M<2> pin to HVCC by switching SW1 to HVCC and close J21 Jumper.
- Force M<1:0> pins to ground by switching SW2 and SW3 to ground.
- Connect HOST FPGA connector on J24.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.

Three devices choices are possible:

- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:

- Close Jumper J25
- Mount a 100k\(\Omega\) resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

*Figure 2-13.* On Board Jumpers, Switches and Connectors
2.6.3 Mode PHY_6_DPDM

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force M<1> pin to HVCC by switching SW2 to HVCC and close J22 Jumper.
- Force M<0> and M<2> pins to ground by switching SW1 and SW3 to ground.
- Connect HOST FPGA connector on J24.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.

Three devices choices are possible:

- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:

- Close Jumper J25
- Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-14. On Board Jumpers, Switches and Connectors
2.6.4 Mode PHY_4_DPDM

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force M<1:0> pins to HVCC by switching SW1 ans SW2 to HVCC. Close J21 and J22 Jumpers.
- Force M<2> pin to ground by switching SW3 to ground.
- Connect HOST FPGA connector on J24.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.
- Three devices choices are possible:
  - Connect Device on J18 Connector
  - or Connect Device on J15 connector
  - or Connect UICC on J10 connector
- For this last device configuration, it is necessary to set the listed jumpers as follows:
  - Close Jumper J25
  - Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
  - Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
  - Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-15. On Board Jumpers, Switches and Connectors
2.6.5 Mode PHY_3_ULPI

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force M<0> and M<2> pins to HVCC. Switch SW1 and SW3 to HVCC. Close J21 and J23 Jumpers.
- Force M<1> pin to ground by switching SW2 to ground.
- Connect HOST FPGA connector on J24.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.

Three devices choices are possible:
- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:
- Close Jumper J25
- Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-16. On Board Jumpers, Switches and Connectors
2.6.6 Mode S7_ICC

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened. Close G1 and G2 Copper Pads.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground. Force OE_N pin to HVCC.
- Force M<1> and M<2> pins to HVCC. Switch SW2 and SW3 to HVCC. Close J22 and J23 Jumpers.
- Force M<0> pin to ground by switching SW1 to ground.
- Connect HOST on connector J1 or J17.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.

Three devices choices are possible:
  - Connect Device on J18 Connector
  - or Connect Device on J15 connector
  - or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:
  - Close Jumper J25
  - Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
  - Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
  - Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

*Figure 2-17. On Board Jumpers, Switches and Connectors*
2.6.7 Mode S7_ICC_BB

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Connect Digital Base Band Reference on TP15 Test Point. (PVRF)
- Close G1 and G2 as specified in the top view below.
- Apply VBUS on P1 pad (VBUS-IN). Close J12 and J16 Jumpers.
- Force OE_\_N pin to HVCC level.
- Force M<1> and M<2> pins to HVCC. Switch SW2 and SW3 to HVCC. Close J22 and J23 Jumpers.
- Force M<0> pin to ground by switching SW1 to ground.
- Connect HOST on connector J1 or J17.

Three devices choices are possible:
- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:
- Close Jumper J25
- Mount a 100k\(\Omega\) resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

*Figure 2-18.* On Board Jumpers, Switches and Connectors
2.6.8 Mode S7_ICC_TK

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount resistors R7 and R8 in order to obtain the expected ratio.
- Close G1 and G2 as specified in the top view below.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force OE_N pin to HVCC
- Force M<1> and M<2> pins to HVCC. Switch SW2 and SW3 to HVCC. Close J22 and J23 Jumpers.
- Force M<0> pin to ground by switching SW1 to ground.
- Connect HOST on connector J1 or J17.
- Apply VBUS on P1 pad (VBUS-IN).
- Three devices choices are possible:
  - Connect Device on J18 Connector
  - or Connect Device on J15 connector
  - or Connect UICC on J10 connector
- For this last device configuration, it is necessary to set the listed jumpers as follows:
  - Close Jumper J25
  - Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
  - Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
  - Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-19. On Board Jumpers, Switches and Connectors
2.6.9 Mode ICC_S7

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 \( \Omega \) resistor on R8. J11 Jumper must be opened.
- Close G1 and G2 Copper Pads.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground.
- Force OE_N pin to HVCC
- Force M<2:0> pins to HVCC. Switch SW1, SW2 and SW3 to HVCC.
- Close J21, J22, J23, J2 and J3 Jumpers.
- Connect HOST on connector J1 or J17.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.
- Two devices choices are possible:
  - Connect Device on J18 Connector
  - or Connect Device on J15 connector

*Figure 2-20.* On Board Jumpers, Switches and Connectors
2.6.10 Mode VCC

First of all, the configuration for this mode means that initially all the jumpers must be removed.

- Mount a 0 Ω resistor on R8. J11 Jumper must be opened. Close G1 and G2 Copper Pads.
- Close J5 Jumper between pin 1 & 2. PVRF must be connected to REFP_LDOH.
- Force Pin1 of the Jumper J12 (VBUS) to ground. Force OE_N pin to HVCC
- Force M<2:0> pins to HVCC. Switch SW1, SW2 and SW3 to HVCC.
- Close J21, J22 and J23 Jumpers.
- Connect Power Supply of the Host on P3 pad and close J14 Jumper.
- Connect Power Supply of the Device on P6 pad and close J13 Jumper.
- Connect HOST on connector J1 or J17.

Three devices choices are possible:
- Connect Device on J18 Connector
- or Connect Device on J15 connector
- or Connect UICC on J10 connector

For this last device configuration, it is necessary to set the listed jumpers as follows:
- Close Jumper J25
- Mount a 100kΩ resistor on R9, R10, R11 and R12 (if necessary).
- Close J6, J7, J8 Jumpers between pin 2 & 3. All nets must be connected to GROUND.
- Close J9 Jumper between pin 1 & 2. C6_SWP must pull-up at PVCC level.

Figure 2-21. On Board Jumpers, Switches and Connectors
2.7 Configuration Pads

A Configuration Pad configures the AT73C260-EK1 Evaluation Board for a custom application. The configuration is programmable by soldering a specific part of the Configuration Pad. To return to the initial configuration, the customer has to solder a short jumper.

Figure 2-22. Configuration Pads with 2 Options

[Diagram showing soldered and unsoldered configurations with labels: Connected, Not connected, Solder, No solder]
Section 3

Technical Specifications

■ System Unit
- Physical Dimensions………………………………………………L= 119.27 mm x W=65.97 mm x H=2.5 mm
- Weight…………………………………………………………………………………………………………………………70 g

■ Operating Conditions
- External Voltage Supply (On HVCC Pad)…………………………………………………………3.3V Typical (3.6V Max)
- External Voltage Supply (On PVCC Pad)…………………………………………………………1.8V / 3.0V Typical (3.6V Max)
- USB Voltage Supply (on VBUS Pad)…………………………………………………………5.0V +/- 5%

■ Connections
- FPGA Communication Connector………………………………………………2x5 pins Header
- Smart Card Reader Connector…………………………………………………….1x10 pins Header
- USB Host Connector…………………………………………………….1 USB Type B / 1 Micro USB Type AB
- USB Device Connector……………………………………………………1 USB Type A / 1 Micro USB Type AB
- Mini Smart Card Connector……………………………………………2x4 pins Contact
Section 4
Schematics

Figure 4-1. AT73C260-EK1 Schematic
5.1 Revision History

Table 5-1. Revision History

<table>
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<th>Document</th>
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<th>Comments</th>
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<td>17-Sep-10</td>
<td>First Issue, 17-Sep-10</td>
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