AT89RFD-08 Reference Design

Hardware User Guide
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Section 1

Introduction

Congratulations on your purchase of the C51 AT89RFD-08 Reference Design. It is designed to give designers a quick start to develop code on the AT89C51SND2C and for prototyping and testing of new designs.

1.1 Overview

This document describes the AT89RFD-08 Reference Design dedicated to the AT89C51SND2C C51 microcontroller. This board is designed to allow an easy evaluation of the product using demonstration software.

To increase its demonstrative capabilities, this stand alone board has numerous serial interfaces (RS232, USB, SPI & TWI) and on-board resources (keyboard & LEDs).

This user guide acts as a general getting started guide as well as a complete technical reference for advanced users.

1.1.1 Typical Applications

- MP3-Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3
**Introduction**

**Figure 1-1. AT89RFD-08 Board**

Power Supply

3V UART

Power Supply Jumper Selection (J14)

Auxiliary Mono Input

Connector

AT89C51SND2

Earphone Jack

Speaker Jack

USB

SPI

Reset

ISP

LED1

LED2

SELECT

OK

Auxiliary Mono Input

Connector

AT89C51SND2

Earphone Jack

Speaker Jack

USB
To complement the evaluation and enable additional development capability, the AT89RFD-08 Board can be connected to a PC (UART) Atmel in order to use the AT89C51SND2C as a slave device.
1.2 AT89RFD-08 Reference Design Features

The AT89RFD-08 Board provides the following features:

- AT89C51SND2C CTBGA device (3V)
- Power supply flagged by “POWER” LED:
  - regulated 3V
  - direct powering from external connector
- ISP connector for on-chip ISP
- Serial interfaces:
  - 1 RS-232 port
  - 1 SPI port
  - 1 TWI port
  - 1 USB port
- On-board resources:
  - 1 earphone 32 Ohms output (jack connector)
  - 1 speaker 8 Ohms output (jack connector)
  - 1 SD/MMC card connector
  - 2-button keyboard
  - 2 LEDs
- On-board RESET button
- On-board INT0 button
- System clock:
  - 16 MHz crystal
- Expansion connector

Note: PC software at89rfd-08-MyCom-X_X.exe is available to control AT89RFD-08. Refer to firmware package readme.txt file.
Section 2

Using the AT89RFD-08 Board

The AT89RFD-08 Board can be used as a stand-alone board or as a slave board.
2.1 Block Diagram

*Figure 2-1. AT89RFD-08 Board Block Diagram*
2.2 Power Supply

The power supply input is performed through the SIP2 connector J1 on top of the board.

*Figure 2-2. Power supply connector*

Once the power is established, the power LED (POWER-ON) is lit.

The on-board power supply circuitry allows various power supply configurations. The power supply selection is performed using J14 jumper.

*Figure 2-3. Power Supply Input Configuration*

To prevent malfunction due to insufficient power supply voltage, we assume that an external brown-out protection or the Master system controls the AT89C51SND2C Reset PIN.

Note: Refer to Atmel Document ‘External Brown-out Protection for C51 Microcontrollers with Active High Reset Input’, available on the Atmel web site.

### 2.2.1 5V to 9V power Supply

J14 shall be configured in the opened position to allow regulation of the power supply to a stable 3V voltage.

*Table 2-1. Regulated Power Supply Configuration*

<table>
<thead>
<tr>
<th>Power supply source</th>
<th>J14(*)</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Power Supply</td>
<td>opened</td>
<td>5</td>
<td>9</td>
<td>V</td>
</tr>
</tbody>
</table>

The power supply voltage is regulated with on board circuitry. Input voltage on this connector should be included between 5 and 9V. This power supply input is protected against polarization inversion.

### 2.2.2 3V power Supply

The direct power supply input can be used when J14 jumper is set closed. This input is used to directly power the board without using the on-board regulator.
Table 2-2. Power supply configuration

<table>
<thead>
<tr>
<th>Power supply source</th>
<th>J14(*)</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Power Supply</td>
<td>closed</td>
<td>2.7</td>
<td>3.3</td>
<td>V</td>
</tr>
</tbody>
</table>

The direct power supply voltage must be adjusted with the power supply source. Input voltage on this connector must be included between 2.7 and 3.3V.

This power supply input is **NOT protected** against polarization inversion.

2.2.3 Power Supply Source Connection

For power supply source connection, there is only the need for a 2 points female connector.

*Figure 2-4.* EXT PWR Female Connector / Cable for 9V Battery

2.2.4 “POWER“ LED

The power LED (“PWR”) is always on when power is applied to the board regardless of power supply configuration.

*Figure 2-5.* “POWER“ LED
2.3 AT89C51SND2C MP3 microcontroller

The microcontroller area consists of the AT89C51SND2C product along with the following items:

- Reset Circuit
- 16 MHz Oscillator
- PLL Filter for USB clock generation

AT89C51SND2C is located in the center of the AT89RFD-08 Reference Design.

*Figure 2-6. Processor Placement*

2.3.1 Reset

2.3.1.1 Power-on RESET

The on-board RC network acts as power-on RESET.

2.3.1.2 RESET Push Button

By pressing the RST push button on the board, a warm RESET of the AT89C51SND2C is performed.

*Figure 2-7. RST Push Button*
2.3.2 CPU Clock

The AT89C51SND2C microcontroller is clocked by a 16MHz crystal (Y1).

*Figure 2-8. Clock Area*

2.3.3 PLL Filter

Generation of the 48MHz clock frequency is based on an internal PLL with its two-capacitors and one-resistor filter.
2.4 Communication Interfaces

2.4.1 RS-232

The AT89C51SND2C features an on-chip UART interface directly wired to SIP3 connector.

Caution: The AT89RFD-08 Board is supplied without any RS-232 driver/receiver. Voltage levels on the RS232 interface shall be compliant with AT89C51SND2C DC characteristics specified in the AT89C51SND2C datasheet.

*Figure 2-9. RS-232 SIP3 Connector*

```
3V UART
```

2.4.2 USB

The AT89RFD-08 Reference Design provides all the required hardware to develop USB compliant application. This includes:

- a USB connector
- a USB unload jumper (J13) which allows to disconnect the pull-up on D+ and then simulate an Attach/Detach of the USB cable.
- a USB VBUS detection capability is given by using P3.3 & P3.4 of the microcontroller

*Figure 2-10. USB Connector*
2.4.3 SPI

The AT89C51SND2C is a micro-controller with an on-chip full duplex SPI interface, master or slave.

A 6-pin male connector assumes the SPI bus connections.

*Figure 2-11.* SPI 6-pin Connector

The SPI 6-pin connector also provides to the user Vcc and Gnd.

*Figure 2-12.* SPI 6-pin Connections

2.4.4 TWI

The AT89C51SND2C provides an on-chip TWI interface, master or slave. The SDA and SCL signals provided for TWI communication are wired to the expansion connector.
2.5 On-board Resources

2.5.1 LEDs

Two LEDs are provided on the AT89RFD-08 Reference Design. They are connected to P2_5 and P2_6 and are all free of usage. No dedicated signaling from the AT89C51SND2C is predefined on these LEDs.

Figure 2-13. LEDs position on the board

2.5.2 2-key Keypad

The AT89RFD-08 board embeds a two-key keypad.

Figure 2-14. Keypad location

SELECT push button is connected to KIN0 line of the microcontroller while OK push button is connected to INT0.

2.5.3 Secure Digital (SD) / MultiMedia Card (MMC) Area

The MultiMedia Card area consists of a single slot connector that allows the plug-in of MMC cards and SD cards.
2.6 Audio Interfaces

2.6.1 Speaker 8 Ohms Output

The speaker area consists of a stereo jack connector connected to the internal amplifier output of the microcontroller.

Note: The Power amplifier output is not protected against short circuit: do not unplug the speaker jack connector while AT89RFD-08 Reference Design is powered to avoid any hazardous short circuit.

2.6.2 Earphone 32 Ohms Output

The earphone area consists of a 32 Ohms stereo jack.

*Figure 2-15. Audio Interfaces*
2.7 Expansion Connector

The expansion area consists of a 20-pin connector.

**Figure 2-16.** JP1 Expansion Connector

![JP1 Expansion Connector Diagram]

**Table 2-3.** Expansion Connector

<table>
<thead>
<tr>
<th>signal name</th>
<th>pin number</th>
<th>signal name</th>
<th>pin number</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1</td>
<td>P3.2</td>
<td>11</td>
</tr>
<tr>
<td>P0.7</td>
<td>2</td>
<td>P3.6</td>
<td>12</td>
</tr>
<tr>
<td>P0.6</td>
<td>3</td>
<td>P3.7</td>
<td>13</td>
</tr>
<tr>
<td>P0.5</td>
<td>4</td>
<td>P2.0</td>
<td>14</td>
</tr>
<tr>
<td>P0.4</td>
<td>5</td>
<td>P2.1</td>
<td>15</td>
</tr>
<tr>
<td>P0.3</td>
<td>6</td>
<td>P2.2</td>
<td>16</td>
</tr>
<tr>
<td>P0.2</td>
<td>7</td>
<td>P2.3</td>
<td>17</td>
</tr>
<tr>
<td>P0.1</td>
<td>8</td>
<td>P2.7</td>
<td>18</td>
</tr>
<tr>
<td>P0.0</td>
<td>9</td>
<td>SDA</td>
<td>19</td>
</tr>
<tr>
<td>VSS</td>
<td>10</td>
<td>SCL</td>
<td>20</td>
</tr>
</tbody>
</table>

2.7.1 Nand Flash connection

The signals provided on the expansion connector make it possible to connect a Nand Flash memory to the board.

**Table 2-4.** Recommended Connection for Nand Flash

<table>
<thead>
<tr>
<th>Expansion connector pin number</th>
<th>Pin name</th>
<th>Nand Flash connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>P3.6</td>
<td>WR#</td>
</tr>
<tr>
<td>13</td>
<td>P3.7</td>
<td>RD#</td>
</tr>
<tr>
<td>14</td>
<td>P2.0</td>
<td>CLE</td>
</tr>
<tr>
<td>15</td>
<td>P2.1</td>
<td>ALE</td>
</tr>
<tr>
<td>16</td>
<td>P2.2</td>
<td>WP#</td>
</tr>
<tr>
<td>17</td>
<td>P2.3</td>
<td>RDY/BUSY</td>
</tr>
<tr>
<td>18</td>
<td>P2.7</td>
<td>CE#</td>
</tr>
</tbody>
</table>
2.8 In-System Programming

2.8.1 ISP Programming
FLIP ISP programming interface can be used to program the microcontroller.

Note: FLIP can be downloaded from ATMEL website.

2.8.2 ISP Using Hardware Conditions
Switch SW1 have to be physically pressed on the board in order to enter this mode. This mode has to be used to upgrade the default firmware.

Figure 2-17. ISP switch location

Before connecting the USB cable for ISP, you must enter USB bootloader to establish the connection with FLIP:

n Press the ISP button.

n Press the RST button while keeping ISP button pressed.

n Release the RST button.

n Release ISP button.

n Connect the USB cable to the AT89RFD-08 Reference Design and to the PC
Microcontroller is now in the ISP mode and is ready to communicate with FLIP.

2.8.3 ISP Using Software Condition
When connected to a PC using a USB cable, the player can be accessed by FLIP software. To enter by software in the ISP bootloader of the player, press ‘Select’ button while the USB cable is plugged into the PC (the ISP software condition are checked only during power ON Reset).

A driver has to be installed the first time (See FLIP installation note). This driver is delivered with ATMEL FLIP software (current version 2.4.0) available on the Web site. When connected, a new device will appear in the hardware window of the PC under the "User interface peripheral" section, named USB_DFU_SND2. See FLIP User’s guide for information about FLIP execution.
2.9 Electrical Parameter Measurement

The AT89RFD-08 Reference Design is designed to enable easy measurement of electrical parameters on the board. 6 configuration pads can be used either for voltage measurements or for current measurements.

2.9.1 Configuration Pad

A configuration pad configures the AT89RFD-08 Board Demo Board for custom application. The configuration is programmable by cutting a specific part (wire) of the configuration pad. To return to the initial configuration, users must solder a short jumper (wrapping wire or solder drop) to replace the cut connection.

*Figure 2-18. Configuration Pad*

2.9.2 AT89C51SND2C Configuration Pads

There are 6 configuration pads are implemented close to the AT89C51SND2C power supply generator:

- n UVDD - USB interface power supply
- n PVDD - PLL power supply line
- n HSVSS - Audio interface reference voltage
- n VDD - Processor digital power supply
- n AUDVDD - Processor analog power supply
- n AUDV р - Audio interface reference voltage

Refer to AT89RFD-08 schematics for configuration pads position.
2.9.3 Measurements

2.9.3.1 Voltage

Voltage measurement shall be done with a CLOSED configuration pad.

*Figure 2-19. Voltage Measurement*

![Voltage Measurement Diagram](image)

2.9.3.2 Current

Current measurement shall be done cutting the configuration pad and connecting a multimeter.

*Figure 2-20. Current Measurement*

![Current Measurement Diagram](image)
2.10 Layout Guide

Signal integrity on Power Supply Decoupling, USB and Audio lines are the main constraints of the PCB.

2.10.1 Power Supply

Considerable care must be taken to provide quiet supplies such as the analog section:
- AUDVREF: Audio Voltage Reference pin for decoupling.
- AUDVCM: Audio Common Mode reference for decoupling.
- AUDVDD, AUDVSS: Audio Digital Supply Voltage and Ground.
- AUDVBAT: Audio Amplifier Supply.
- UVDD, UVSS: USB Supply Voltage.
- PVDD, PVSS: PLL Supply voltage and Ground.

and digital section:
- VDD and VSS: Digital Supply Voltage and Ground.

Power Supply rails must be routed in ‘star’ in order to reduce as much as possible the noise in the lines. The common point of the power supply lines must me as close as possible of the regulator output.

Each of these power supplies shall have decoupling capacitors.

Power Supply Implementation:
- All power sources wires can carry up to 500 mA
- All Power supply types must have at least one test point access on the Bottom side of the board for test (it can be limited to a single padstack)
- Input and Output filter capacitors must be placed as close as possible from the Voltage Regulator
- Care must be taken on the routage of the power supply (star routage, local ground copper area...)
- The filter tantalum capacitors must have a low ESR.
- The Voltage Regulator must be placed on the component side and above a copper pad linked VDD.Decoupling

The role of the decoupling is to maintain stable the power-supply. In other word, if the frequency domain is considered, the decoupling maintains low the impedance across the power-supply pins of the device in order to short circuit the harmonics of the current which are contains in the disturbances.

The decoupling capacitors must me as close as possible of the microprocessor.

Priority is given to placement enabling the shortest wiring.
2.10.2 USB

The UVDD line must be large enough to drive 500mA.

The D+ and D- lines must be routed side by side because they are a differential pair. There must be two UVSS lines on each side of this two lines.

USB serial resistors 27 ohms on D+ and D- lines must be placed as close as possible of the processor.

2.10.3 Audio

Resistance on the power supply lines and audio lines should be lower than 100 mOhms, especially for:

- Headset Output (Audio Channel Headset Driver Output HSL and HSR).
- Power Amplifier Output. HPP and HPN signals must be routed side by side because they are a differential pair.
2.11 FAQ

1. Can the decoupling capacitors for AUDVCM, CBP and AUDVREF be changed?

   Lowering the decoupling capacitors increases the noise (due to power supply rejection) in low frequency (i.e. dividing the capacitor value by 2 increases the noise by 2 in low frequency). Raising the decoupling capacitors increases the start-up time (due to the charge of the capacitor through their resistive biasing).

   A tolerance value of +/-10% for all these capacitors is recommended (the variation of the noise performances will be negligible).

2. Is it possible to use a 6.5W load impedance for the PA?

   Yes, it is possible to use it at the expense of a THD degraded (some dB) and higher power dissipation. (25% raised with a 20% lower load impedance). Refer to product datasheet plot maximum dissipated power versus power supply and impedance load.

3. The capacitors for the Headset 100uF are too big, can I change their value?

   These capacitors set the cutting frequency. With 32W load, cutting frequency Fc is:
   \[ F_c = 1/(2 \pi R_{LOAD} C) \]

   The effective power is given by the following formula:
   \[ P_{EFF\,MAX} = (1.2 / 1.414)^2 / R_{LOAD} = 0.72 / R_{LOAD} \ [W \ Rms] \]

   **Figure 2-21.** Headset Output

   ![Headset Output Diagram]

   **Table 2-5.** Cutting Frequency Versus Effective Power

<table>
<thead>
<tr>
<th>Capacitor C (mF)</th>
<th>Load Resistance (Ohms)</th>
<th>Cutting Frequency (Hz)</th>
<th>Effective Power (mW Rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>32</td>
<td>50</td>
<td>22.5</td>
</tr>
<tr>
<td>22</td>
<td>32</td>
<td>226</td>
<td>22.5</td>
</tr>
<tr>
<td>10</td>
<td>32</td>
<td>497</td>
<td>22.5</td>
</tr>
</tbody>
</table>

   It is possible to add a serial resistor Rs between R_{LOAD} and AUDVSS, to increase the cutting frequency but in this case, it decreases the maximum effective power in the Load.
Using the AT89RFD-08 Board

Figure 2-22. Headset Output when adding serial resistor Rs

![Diagram of headset output](image)

Cutting Frequency is now:

\[ F_c = \frac{1}{2\pi (R_{LOAD} + Rs)C} \]

The effective power is now given by the following formula:

\[ P_{EFF \, MAX} = \frac{0.72 \cdot R_{LOAD}}{(Rs + R_{LOAD})^2} \, [W \, Rms] \]

Table 2-6. Cutting Frequency Versus Effective Power when adding Rs

<table>
<thead>
<tr>
<th>Capacitor C (mF)</th>
<th>Load Resistance Rs + R_{LOAD} (32+96 Ohms)</th>
<th>Cutting Frequency (Hz)</th>
<th>Effective Power (mW Rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>128</td>
<td>12</td>
<td>1.4</td>
</tr>
<tr>
<td>22</td>
<td>128</td>
<td>57</td>
<td>1.4</td>
</tr>
<tr>
<td>10</td>
<td>128</td>
<td>124</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Note: When adding the serial resistor Rs, attenuation is: \(20 \cdot \log\frac{R_{LOAD}}{Rs + R_{LOAD}}\) = -12 dB.

4. I don’t use HSL and HSR, can they stay unconnected?

HSR HSL can stay unconnected if not used and not activated.

5. Regarding the AT89RFD-08 schematics, I want to use 2.7 V for AT8xC51SND2C instead of 3V, and AUDVBAT connected to battery 3.6V, is it possible?

Yes, it is possible but AT8xC51SND2C power supply shall be at least 3V for USB operation to comply USB specification. In this case, you can use the power supply schematic described below.

Note: The schematic refer to Sipex SP6231EN-3: 500mA, 3.3V Linear Regulator with Auxiliary Backup. The SP6231 is a 500mA, 3.3V LDO with an integrated auxiliary voltage input switch. During normal operation, the SP6231 acts as a standard LDO with an output voltage of 3.3V delivering up to 500mA. When the USB VBUS 5V input drops below 4.4V, the 3.3V, VAUX input is switched to the output through an internal PFET, maintaining a constant “glitch free” output voltage.
Note: To prevent any malfunctions during periods of insufficient power supply voltage, AT89C51SND2C voltage supply shall be monitored by a voltage supervisor. During USB operation, AT89C51SND2C voltage supply shall be 3.0V to 3.6V to comply USB specification. AUDVBAT (audio power amplifier supply) can be connected to Battery (at least 3.0V).

6. How can I connect the LINEL and LINER to a stereo input?

**Figure 2-24.** Line-In Connection
7. How can I connect the AUXN and AUXP to a mono input?

Figure 2-25. Mono Input Connection

8. How should I connect and manage AT8xC51SND2C reset and power supply?

AT8xC51SND2C have to be maintained under reset during power-on and power-off sequences.

AT8xC51SND2C power supply power-up:
- 0V to 1V: don't care.
- 1V to VDD: AT8xC51SND2C have to be maintained under reset to prevent any flash corruptions and hazardous behavior.

AT8xC51SND2C Power supply power-off:
- VDD to 1V: AT8xC51SND2C have to be maintained under reset to prevent any flash corruptions (Flash version only) and hazardous behavior.
- 1V to 0V: don't care.

To verify the effectiveness of the solution, please ensure that ALE signal (to enable in software) must not toggle during these sequences.

Note: To prevent system malfunctions during periods of insufficient power supply voltage, AT8xC51SND2C voltage supply shall be monitored by a voltage supervisor. Refer to Atmel Document 'External Brown-out Protection for C51 Microcontrollers with Active High Reset Input'.

How shall I drive the NandFlash WP/ IO if I do not want to connect to the AT8xC51SND2C?
9. What about power through I/O pins as RxD, TxD if AT8xC51SND2C is not powered?

The AT8xC51SND2C can have an unexpected behavior if Powered through IOs:
- consumption.
- microcontroller can execute the code.

Solutions:
- Use AT8xC51SND2C Reset Pin (no code execution but extra consumption).
- Use AT8xC51SND2C in power down mode (Power supply needed).

AT8xC51SND2C shall not be powered through I/O pins if there is no power supply.
10. How can I improve the USB VBUS detection to avoid the power through I/O if AT8xC51SND2C is not powered?

You can use the VBUS detection described in AT89RFD-08 schematics.

11. Can I connect AT8xC51SND2C reset pin to a Controller GPIO?

You can use the following schematic:

![Schematic](image)

12. What is the effect to change the INGND, CBP, AUDVREF, AUDVCM capacitor values?

- **INGND** is the reference input of the LINE_IN input stages. Should be chosen equal to two times the input LINE_IN capacitors. For a full audio bandwidth, Zin_min=9kOhms, Cin=1uF, INGND capacitor =2.2uF recommended. For a vocal-range bandwidth, Cin=100nF, INGND capacitor =220nF (for a 200Hz cut-off frequency).

- **CBP** capacitor value: This is the decoupling capacitor of the internal half-supply reference of the power amplifier. 100nF are recommended. Should be reduced down to 10nF for a vocal-range usage (300-3000 Hz bandwidth).

- **AUDVREF** capacitor: Decoupling capacitor of the reference of the DAC. 10uF is mandatory to insure a proper reference. It should not be reduced.

- **AUDVCM** capacitor: Decoupling capacitor of the common mode reference of the headset/line-out amplifiers, the common mode reference of the MONO PA driver, the common-mode reference of the LINE_IN input stages, the common mode reference of the AUX input stage, and the common mode reference of the DACs. Can not be reduced, in order to insure proper references.

13. Shall I add a high pass filter to avoid noise on PA output (<1KHz)?

It is possible to change the capacitors of PA input (PAINP, PAINN) to adjust the low cutting frequency. The input impedance also depends on the selected gain:

\[
F(-3 \text{ dB}) = \frac{1}{2 \pi C Z}\]

where \(C\) is the capacitor value and \(Z\) the PA input impedance.

**Table 2-7.** PA Gain / Zin

<table>
<thead>
<tr>
<th>PA Gain (dB)</th>
<th>PA Zin (ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>15 K</td>
</tr>
<tr>
<td>17</td>
<td>21 K</td>
</tr>
<tr>
<td>14</td>
<td>27 K</td>
</tr>
<tr>
<td>11</td>
<td>36 K</td>
</tr>
</tbody>
</table>
Example with \( F_c = 100 \text{ Hz}, \) \( \text{PA Gain} = +5 \text{ dB} \Rightarrow \text{Cin} = 27 \text{ nF} \)

For low frequency noise rejection, internal mechanism is a full differential mode, and decoupling with common mode (capacitor CBP).

### 14. What are the PA impedance in power-off?
- Between PAINP and HPN (or LPHN): 165 K ohms.
- Between PAINN and HPP (or LPHN): 165 K ohms.
- Between HPP and HPN: 10 K ohms.
- Between HPP and LPHN: 10 K ohms.

### 15. What will be the AT8xC51SND2C power supply during USB mass storage mode?

The AT8xC51SND2C power supply (VDD, UVDD, PVDD) shall be \( > 3 \text{ V} \) to comply USB specification (output level voltage on D+/D-).

If USB certification is not required, it is possible to have 2.8V for VDD, UVDD, PVDD, but the D+ pull-up (controlled by PNP transistor) shall be connected to a voltage \( > 3 \text{ V} \).

**Note:** Refer to USB chapter 7 [http://www.usb.org/developers/docs](http://www.usb.org/developers/docs)

<table>
<thead>
<tr>
<th>PA Gain (dB)</th>
<th>PA Zin (ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>46.5 K</td>
</tr>
<tr>
<td>5</td>
<td>60 K</td>
</tr>
<tr>
<td>2</td>
<td>72 K</td>
</tr>
<tr>
<td>-1</td>
<td>87 K</td>
</tr>
<tr>
<td>-4</td>
<td>100.5 K</td>
</tr>
<tr>
<td>-7</td>
<td>114 K</td>
</tr>
<tr>
<td>-10</td>
<td>126 K</td>
</tr>
<tr>
<td>-13</td>
<td>135 K</td>
</tr>
<tr>
<td>-16</td>
<td>142.5 K</td>
</tr>
<tr>
<td>-19</td>
<td>148.5 K</td>
</tr>
<tr>
<td>-22</td>
<td>153 K</td>
</tr>
</tbody>
</table>
16. How shall we avoid modulation / distortion on audio output when decoding MP3?

Please take care of the digital volume of the MP3 decoder (MP3VOL register). When MP3VOLL and MP3VOLR are set to maximum (1Fh), it is possible to have modulation for a 0 dB sinus.

For testing audio output from sinus wave, use the default settings for MP3VOLL(0Fh) and MP3VOLR (0Fh) (MP3 decoder digital volume) and adjust the LINE_OUT gain to get 0dB on full chain.

In AT89RFD-08 firmware, it is possible to send the AUDIO_SET_GAIN (Line_out, 00h) command (7Eh FFh 91h 02h 00h 00h 92h).

17. Could you please confirm the difference between 0dBFS (Full Scale) and zero? (target characteristic is over 85dB.)

"Zero" has no signification. For SNR and THD parameters of the DAC, they are referred to its full scale (dBFS). In the DAC specification, SNR and THD are given for a -1dBFS level.

For the SNR, the Headset amp should be loaded with a 32 Ohms resistor (headphone specification)

Coupling capacitor value: 100uF.

Test equipment: AUDIO PRECISION system Two 2322 for example or FFT Bandwidth 20KHz, A weighting.

Test Condition:
- DAC Gain (DAC_RLOG,DAC_LLOG) = 0 dB => AUDIO_SET_GAIN command for DAC (00h).
- PA Gain (in PA_CTRL) = 0 dB => AUDIO_SET_GAIN command for PA (01h).
- Output load on Headset (HSR,HSL) = 10Kohms.
- Play a 1KHz -3 dB sinus MP3 on DAC.

18. How can I test the distortion characteristic on headset?

This distortion depends on load impedance: typical 32 ohms.

Use a 32 Ohms load (through a 100uF coupling capacitor)

Input signal: pure sine wave, level -1dBFS, frequency 1KHz

THD spec: -65dB typ, -60dB max

Test equipment: AUDIO PRECISION system Two 2322 for example or FFT Bandwidth 20KHz, A weighting.

19. Could you confirm the frequency characteristic on headset? (Headset capacitors value are not yet defined)

The low frequency cut-off is determined by the capacitive coupling with the load. With a 100uF capacitor and a 32 Ohms load, the frequency cut-off is about 50Hz.
The high frequency cut-off is essentially determined by the DAC digital filter response (and hence its clock frequency). This frequency is 0.4535Fs, Fs the sampling frequency (i.e. 44.1KHz).

20. Confirm the isolation between L-channel and R-channel of headset line.
The specification is 80dB @1KHz. Note it is very sensitive to the environment (PCB). Please use ground planes; capacitive coupling between the two outputs has to be reduced to its minimum.
Section 3

Technical Specifications

n System Unit
- Physical Dimensions ........................................... L=100 x W=100 x H=27 mm
- Weight ........................................................................................................... 70 g

n Operating Conditions
- Voltage Supply ........................................................................ 2.7V - 3.3V or 5V - 9V

n Connections
- RS 232C Connector ................................................................. 3-pin SIP connector
- RS 232C Communications Maximum Speed ......................... 500 kbps
- SPI Connector ............................................................................. 6-pin SIP connector
- SPI Communications Maximum Speed ................................. 4 Mbps
- TWI Connector ........................................................................ expansion connector
- TWI Communications Maximum Speed ............................... 400 kbps
Section 4
Technical Support

For Technical support, please contact mcu@atmel.com. When requesting technical support, please include the following information:

- Which target C51 device is used (complete part number)
- Target voltage and speed
- Clock source and fuse setting of the C51
- Programming method (ISP or specific Boot-Loader)
- Hardware revisions of the tools
- Version number of FLIP
- PC operating system and version/build
- PC processor type and speed
- A detailed description of the problem